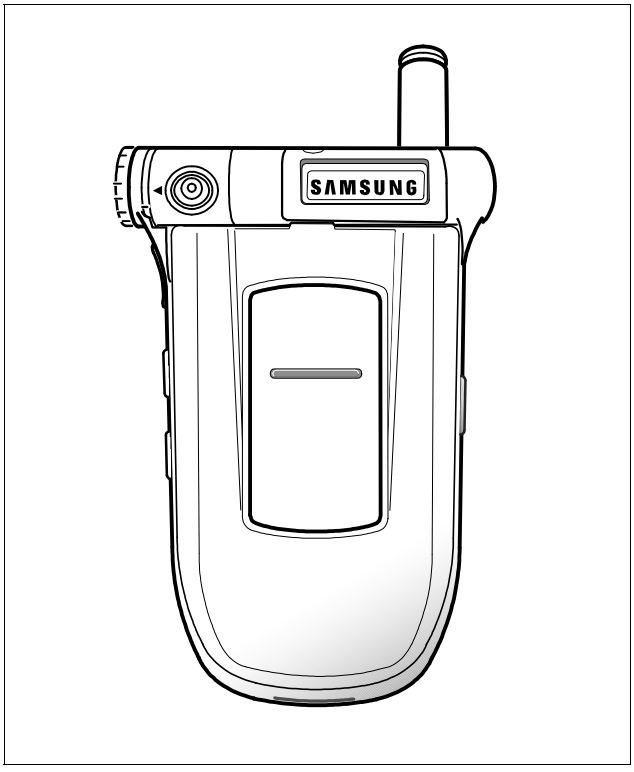
SAMSUNG

GSM TELEPHONE
SGH-P400

SERVICE Manual

GSM TELEPHONE



CONTENTS

1. SGH-P400 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1	PCS1900
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880	1850~1910 1930~1990
ARFCN range	1~124	0~124 & 975~1023	512~885	512~810
Tx/Rx spacing	45MHz	45MHz	95MHz	80MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm	-100dBm
TDMA Mux	8	8	8	8
Cell Radius	35Km	35Km	2Km	-

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2. GSM TX power class

TX Power control level	GSM900
5	33±2 dBm
6	31±2 dBm
7	29±2 dBm
8	27±2 dBm
9	25±2 dBm
10	23±2 dBm
11	21±2 dBm
12	19±2 dBm
13	17±2 dBm
14	15±2 dBm
15	13±2 dBm
16	11±3 dBm
17	9±3dBm
18	7±3 dBm
19	5±3 dBm

TX Power control level	DCS1800
0	30±3 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

TX Power control level	PCS1900
0	30±3 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

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2. SGH-P400 Circuit Description

1. SGH-P400 RF Circuit Description

1) RX PART

1. ASM(U1005)
   ⇨ 510Switching Tx, Rx path for GSM900, DCS1800 and PCS1900 by logic controlling.

2. ASM Control Logic (U701, U702, U703)
   ⇨ Truth Table

	VC1	VC2	VC3
GSM Tx Mode	H	L	L
DCS /PCS Tx Mode	L	H	L
PCS Rx Mode	L	L	H
GSM / DCS Rx Mode	L	L	L

3. FILTER
   To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

   - GSM FILTER (C1003,C1004,L1001)
     ⇨ For filtering the frequency band between 925 ~ 960 MHz

   - DCS FILTER (C1005,C1006,L1002)
     ⇨ For filtering the frequency band 1805 and 1880 MHz.

   - PCS SAW FILTER (F1003,C1009,C1010,L1006)
     ⇨ For filtering the frequency band between 1930 and 1990 MHz

4. TC-VCXO (OSC801)

   To generate the 13MHz reference clock to drive the logic and RF.
   After additional process, the reference clock is applied to the U900 Rx IQ demodulator and Tx IQ modulator.
   The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

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5. Si 4200 (U901)

This chip integrates three differential-input LNAs.
The GSM input supports the E-GSM, DCS input supports the DCS1800, PCS input supports the PCS1900. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.
Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from SI4133T frequency synthesizer.
The RFLO frequency is between 1737.8 ~ 1989.9 MHz.
The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.
The quadrature IF signal is digitized with high resolution A/D converts (ADC).

6. Si 4201 (U900)

The SI4201 down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal.
Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals. After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U902 chip.
SI4200 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U1001).
The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below,

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

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2. Baseband Circuit description of SGH-P400

1) PSC2106 & LTC 1734

1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life.
A programmable boost converter provides support for 1.8V, and 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as an LED driver and two call-alert drivers, aid in reducing both board area and system complexity.
A three-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the PSC2106 and enables system designers to maximize both standby and talk times.
Supervisory functions. including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

2. Battery Charge Management

A battery charge management block provides fast, efficient charging of a single-cell Li-ion battery. Used in conjunction with a current-limited voltage source and an external PMOS pass transistor, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

3. Backlight LED Driver

The backlight LED drivers are low-side, programmable current source designed to control the brightness the keyboard and LCD illumination. LED1_DRV is controlled via LED1_[0:2] and can be programmed to sink from mA to 60mA in 7.5mA steps. LED2_DRV is controlled via LED2_[0:2] and can be programmed to sink from 5 to 40mA in 5mA steps. Both LED drivers are capable of sinking their maximum output current at a worst worst case maximum output voltage of 0.6V. For efficient use, the LEDs should be forward connected between the ma battery and their corresponding LED driver output.

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2) Connector

1. LCD Connector

LCD is consisted of main LCD(color 65K TFD LCD). Chip select signals of EMI part in the trident, CAM_CLCD_EN,
can enable main LCD. LED_EN signal enables white LED of main LCD. This signal is from IO part of the DSP in the trident. RST signal from 2106 initiates the initial process of the LCD.
16-bit data lines(D(0)~D(15)) transfers data and commands to LCD through emi_filter. Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So CP_WEN signal is used to write data or commands to LCD.
Power signals for LCD are V_bat and V_ccd.
SPK1P and SPK1N from CSP1093 are used for audio speaker. And VIB_EN from enables the motor.

2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'.
CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

3. IRDA

This system uses IRDA module, HSDL_3201, HP's. This has signals, IRDA_EN(enable signal), IRDA_RX(input data) and IRDA_TX(output data). These signals are connected to PPI of trident. It uses two power signals. V_ccd is used for circuit and V_bat is used for LED.

3) IF connetor

It is 18-pin connector. They are designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, VEXT, VTEST, VF, CF, VBAT and GND. They connected to power supply IC, microprocessor and signal processor IC.

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4) Audio

AOUTAP from CSP1093 is connected to the main speaker. AOUTAN is connected to the speaker via audio-amp. AOUTBN and AOUTBP are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.

YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.
As a synthesis, YMU762MA3 is equipped 16 voices with differenttones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects.
Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexiblysupport application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.
YMU759 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor and a circuit for controlling LEDs synchornous with music.
For the headphone, it is provided with a stereophonic output terminal.
For the purpose of enabling YMU762MA3 to demonstarte its full capablities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible wiht multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for traning karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to systhesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

The vibrator motor driver is a low-side, programmable voltage source designed to drive a small dc motor that silently alerts the user of an incoming call. The driver is enabled by EN_VIB, and its voltage setting is determined by VIB[0:2]. Provided EN_VIB is a logic 1, the driver can be programmed to maintain a

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motor voltage of 1.1V to 2.5V in 20mV steps and while sinking up to 100mA. For efficient use, the vibrator motor should be connected between the main battery and the VIB_DRV output.

5) Memory

This system uses SHARP's memory, LRS1828A.
It is consisted of 128M bits flash memory and32M bits psuedo SRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP1093. It has 22 bit address lines, A[1~22]. They are connected too. CP_CSROMEN and CO_CSROM2EN signals, chip select signals in the trident enable two memories. They use 3 volt supply voltage, V_ccd and 1.8 volt supply voltage, Vcc_1.8a in the PSC2106. During wrting process, CP_WEN is low and it enables writing process to flash memory and pseudo SRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or SRAM to data lines. Each chip select signals in the trident select memory among 2 flash memory and 2 SRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use FLASH_RESET, which is buffered signal of RESET from PSC2106, for ESD protection. A[0] signal enables lower byte of pseudo SRAM and UPPER_BYTE signal enables higher byte of pseudo SRAM.

6) Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACC(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface.
DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP1093. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU759. ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.
CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.

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Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communicatios using IRDA(IRDA_RX/TX/EN) and data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR). And UP_CS/SCLK/SDI, control signals for PSC2006 are outputted through PPI pins. It has signal port for charging(CHG_DET, CHG_STAT0), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD and small LCD with DSP IP pins.

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7) CSP1093

CSP1093 integrates the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions. The CSP1093 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP1093's internal register, and program CSP1093's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP1093's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP1093 then notifies the DSP which has ample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

8) X-TAL(13MHz)

This system uses the 13MHz TCXO, TCO-9141B, Toyocom. AFC control signal form CSP1093 controls frequency from 13MHz x-tal. It generates the clock frequency. This clock is fed to CSP1093,Trident,YMU759 and Silab solution.

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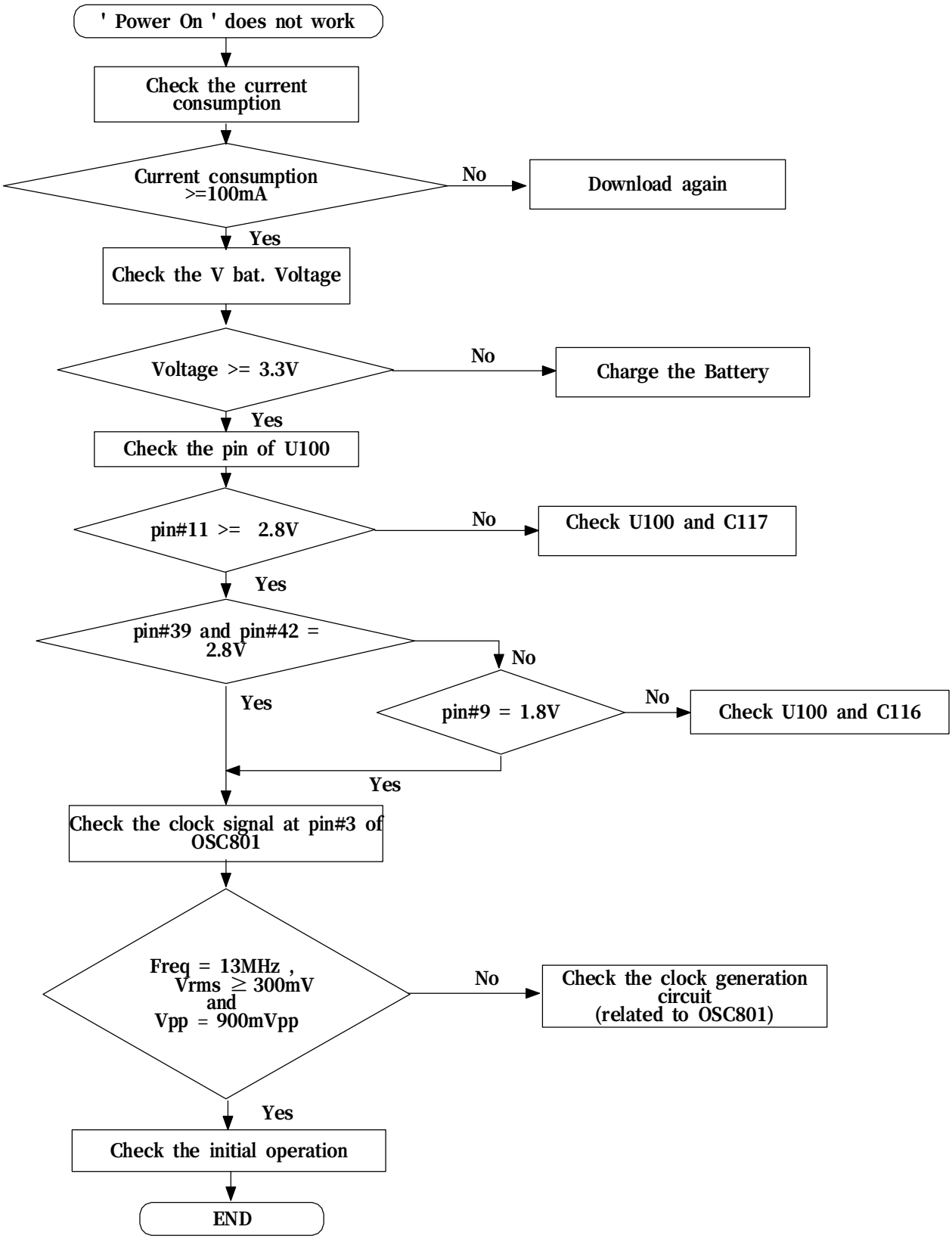
3. SGH-P400 Flow Chart of Troubleshooting

1. Power On



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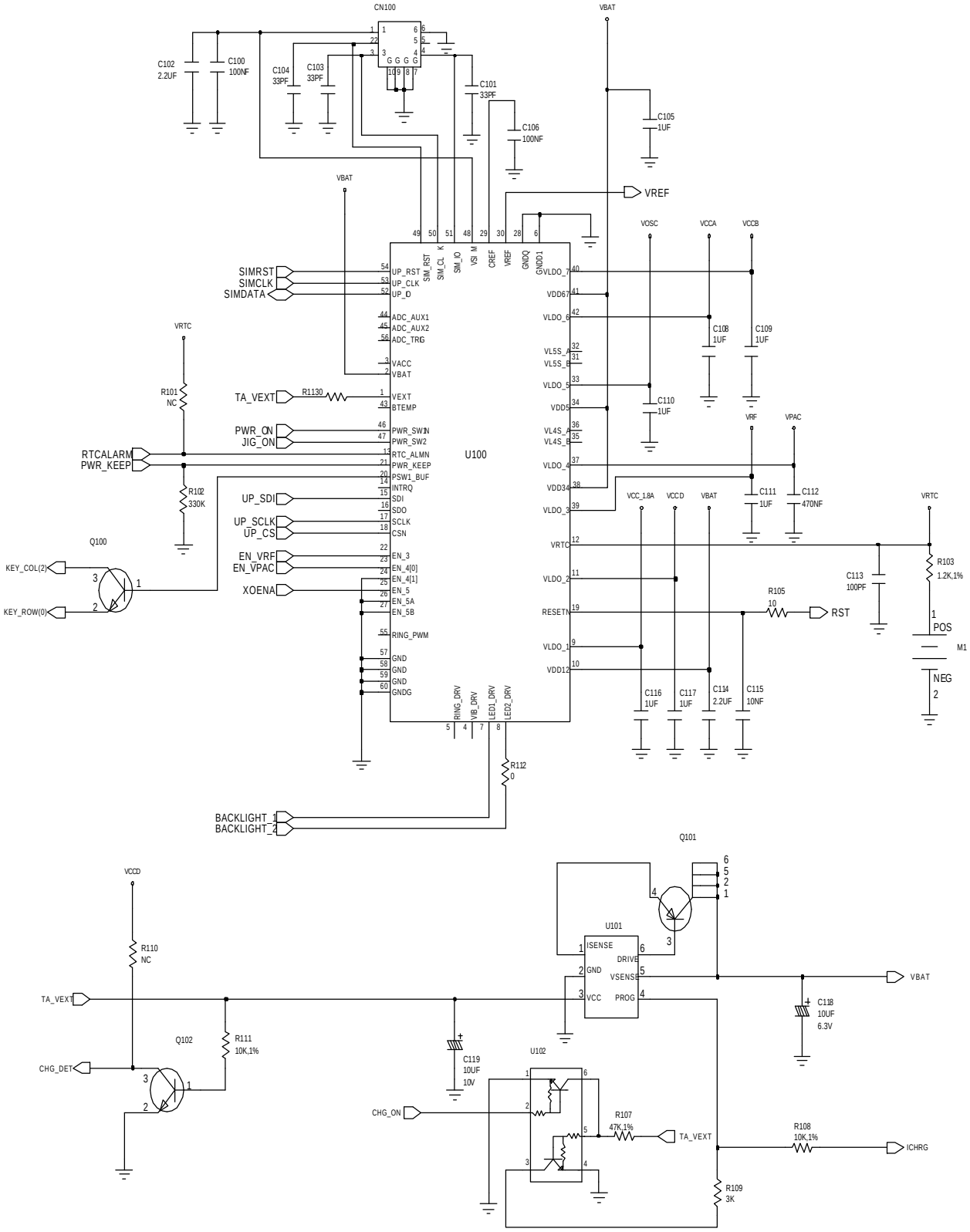

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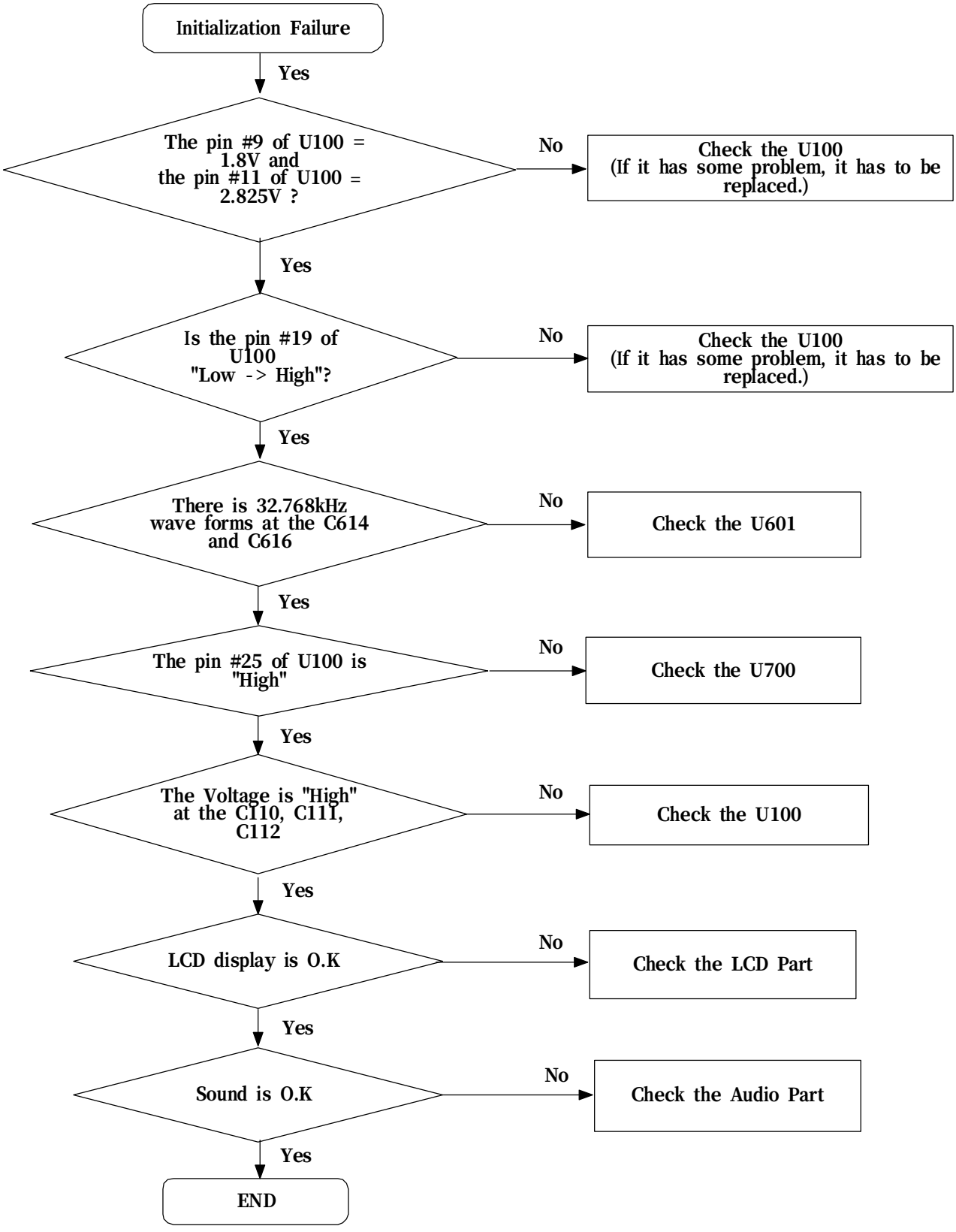
2. Initial



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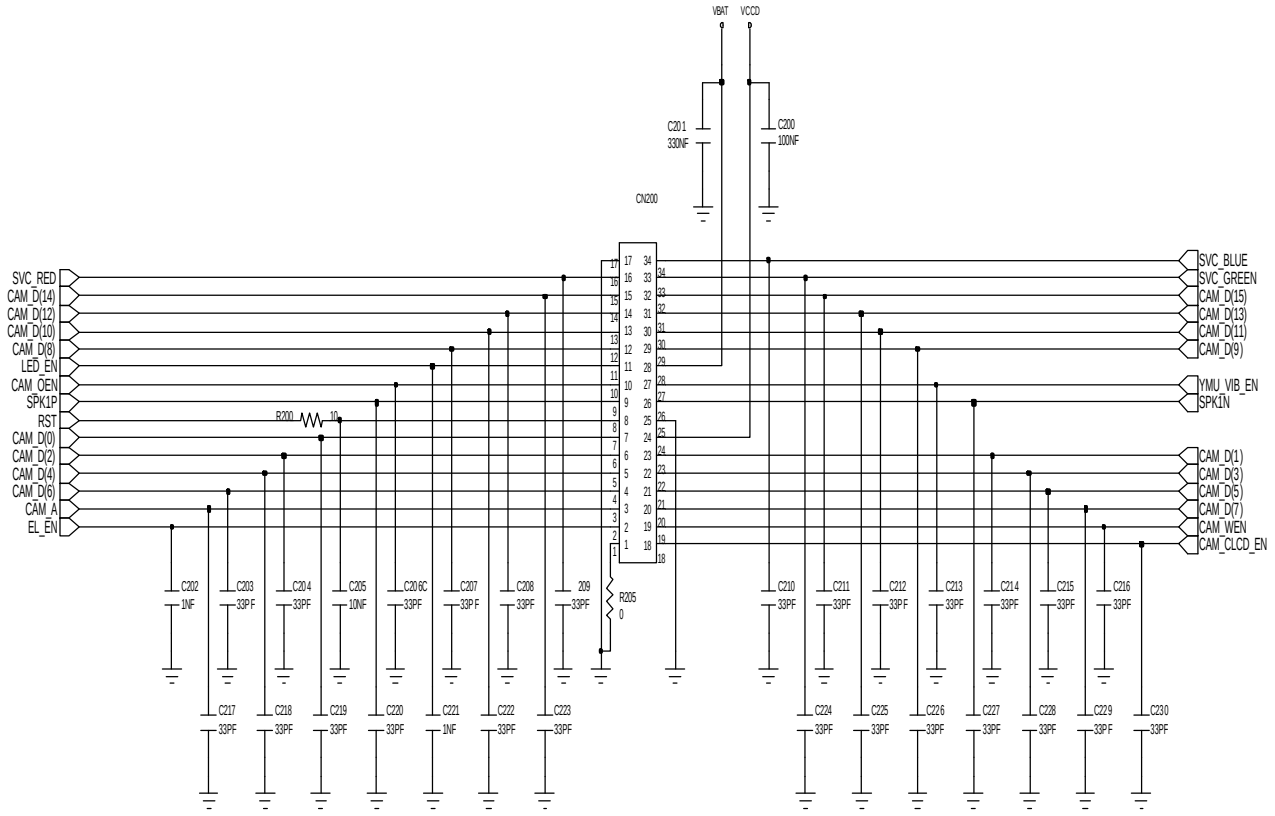

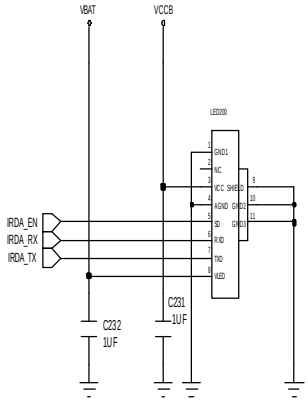

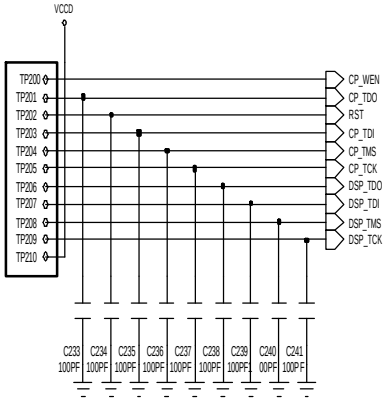

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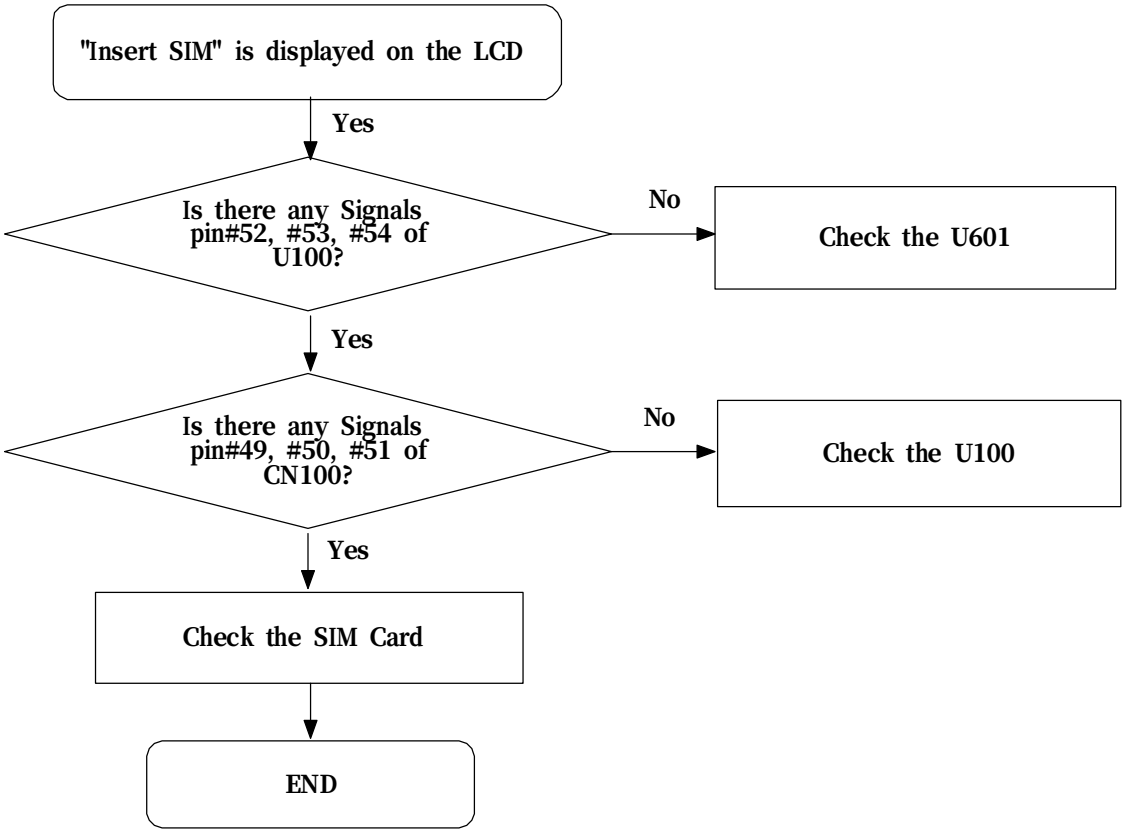
3. Sim Part



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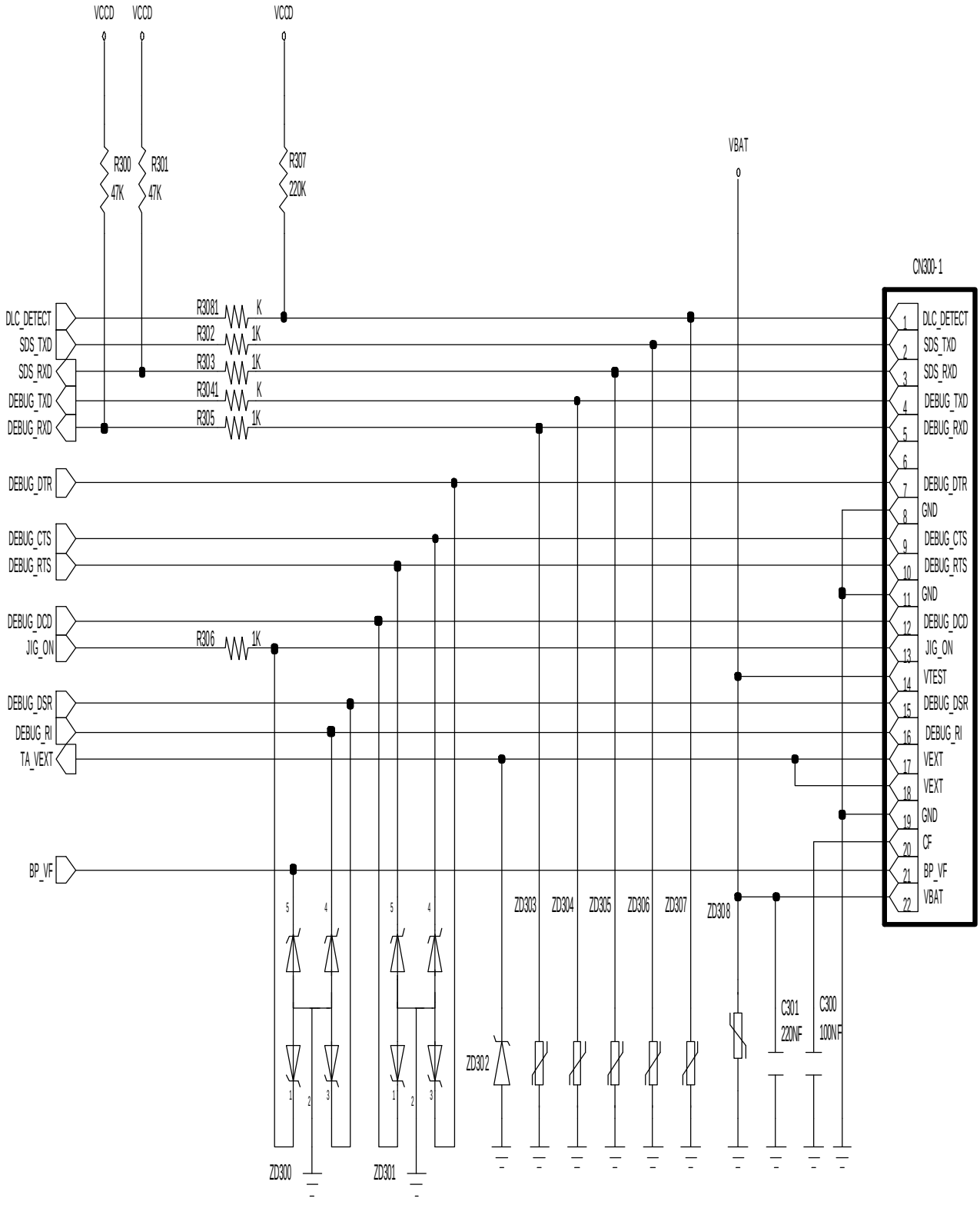

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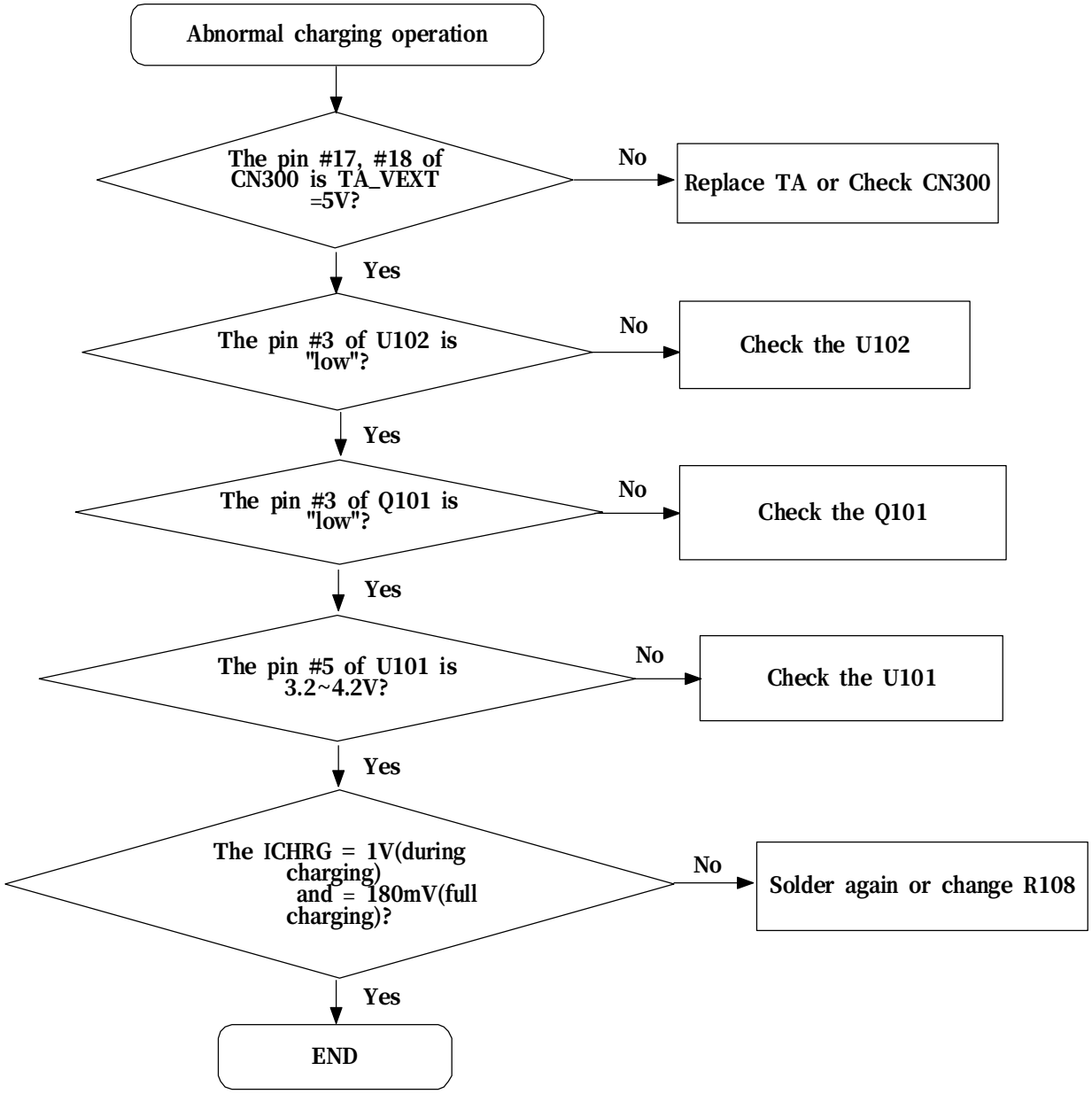
4. Charging Part



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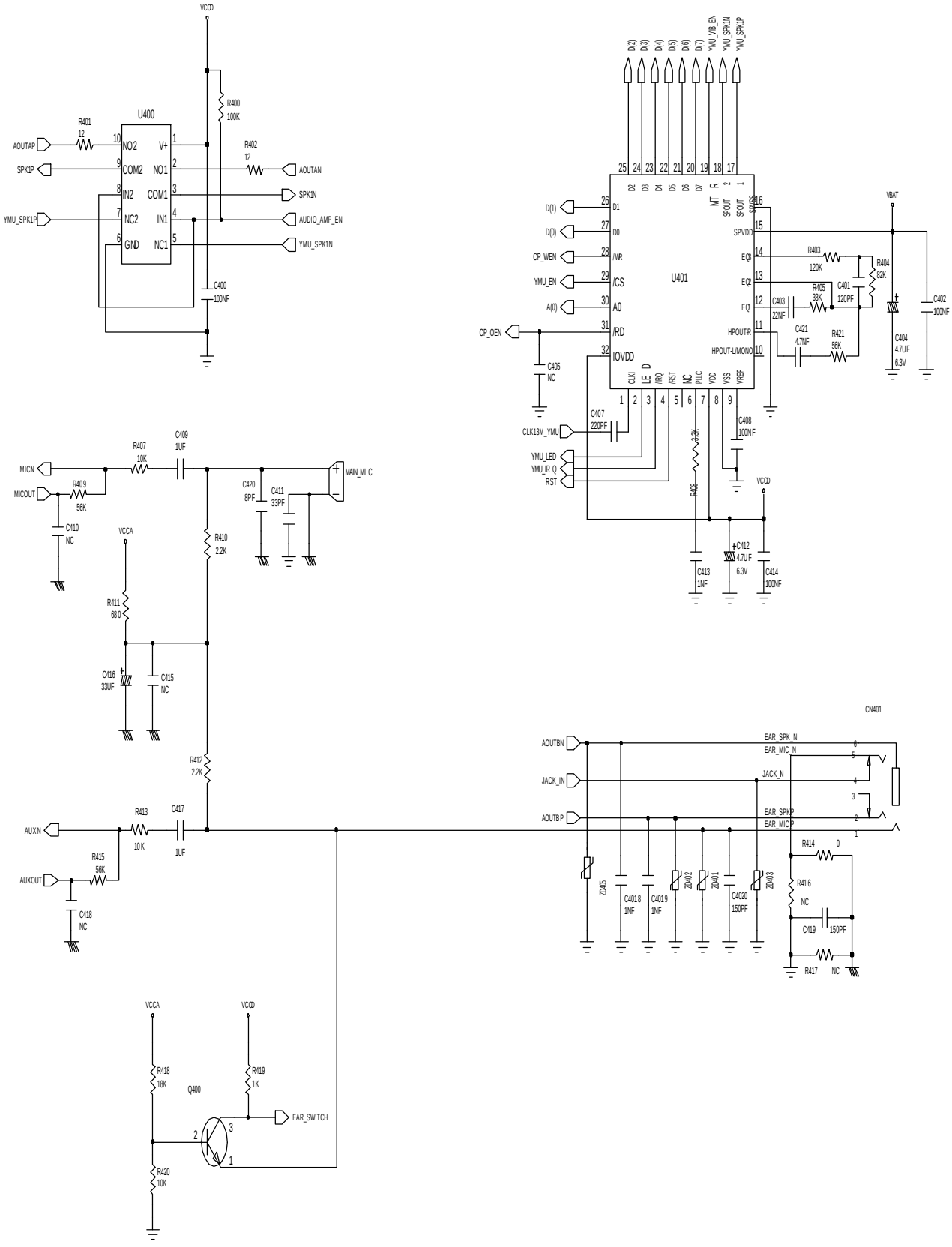

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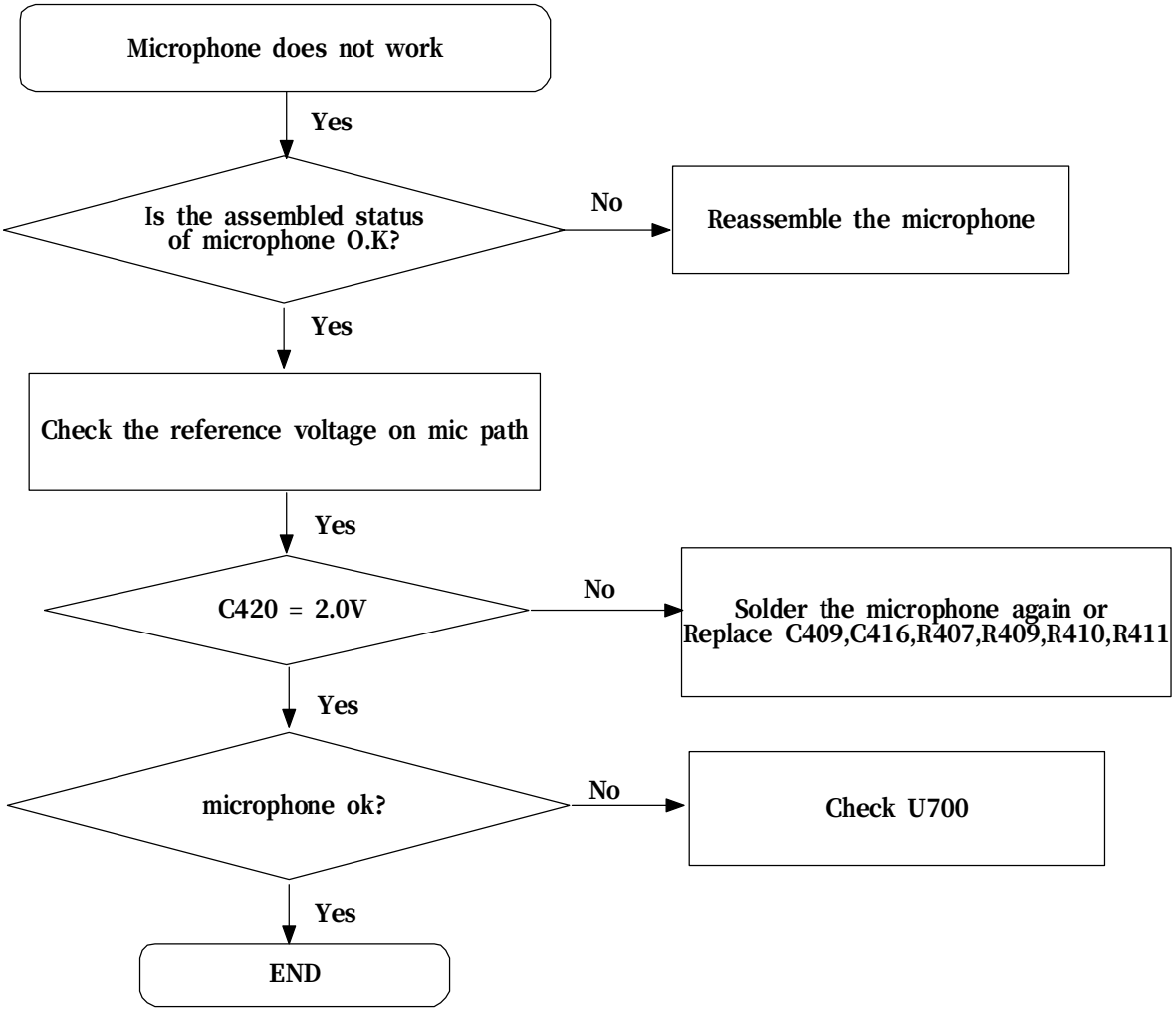
5. Microphone Part



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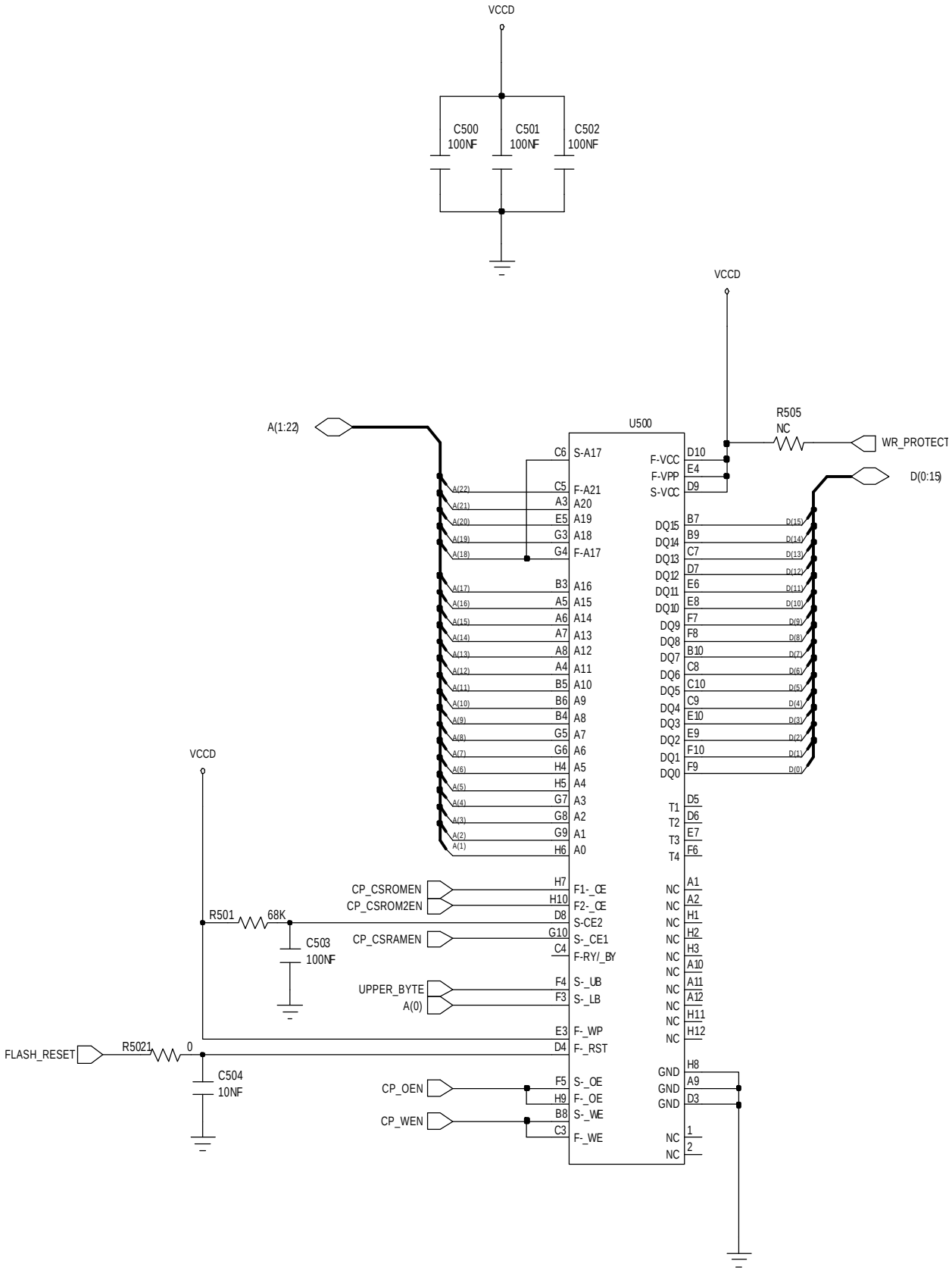

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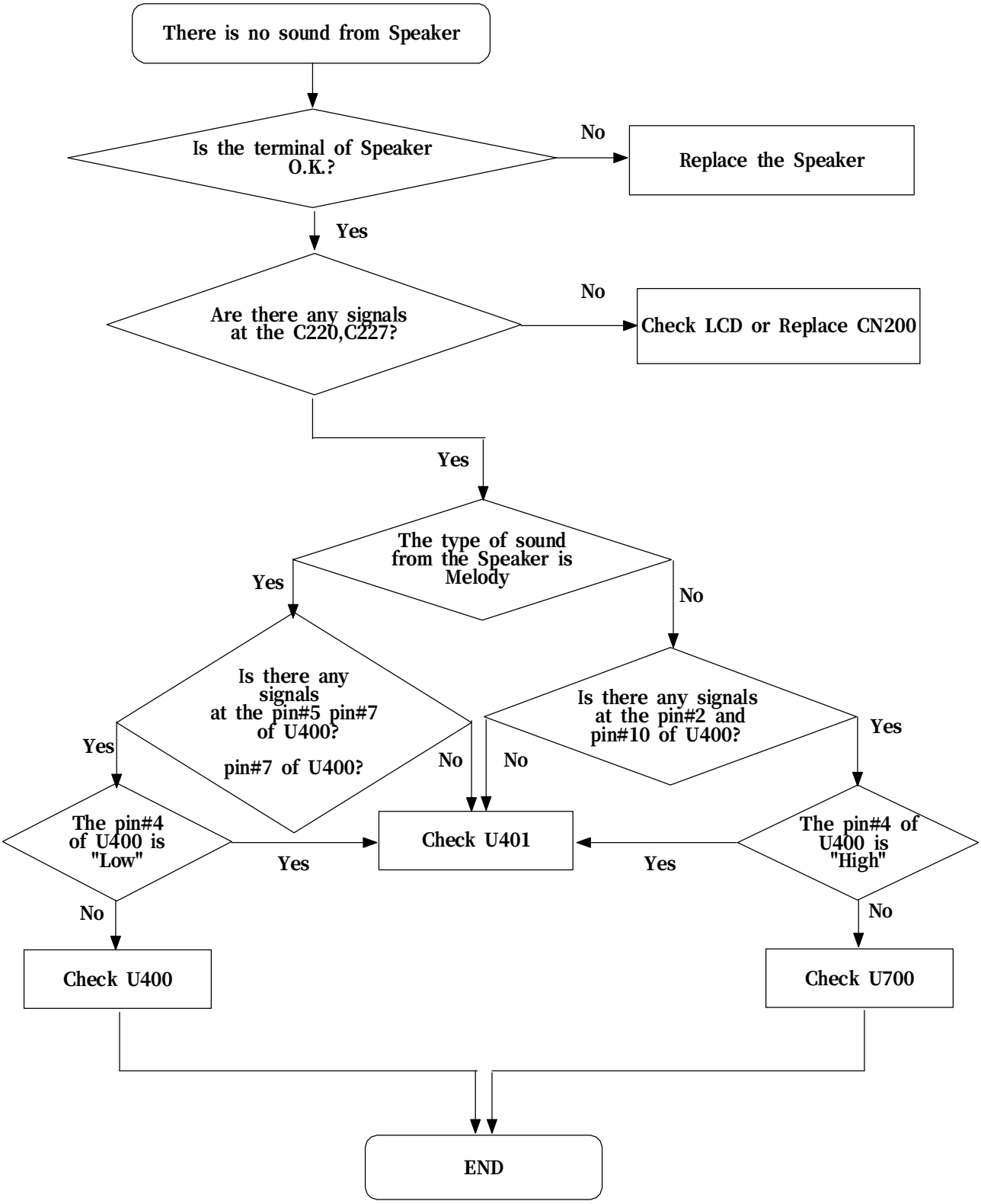
6. Speaker Part



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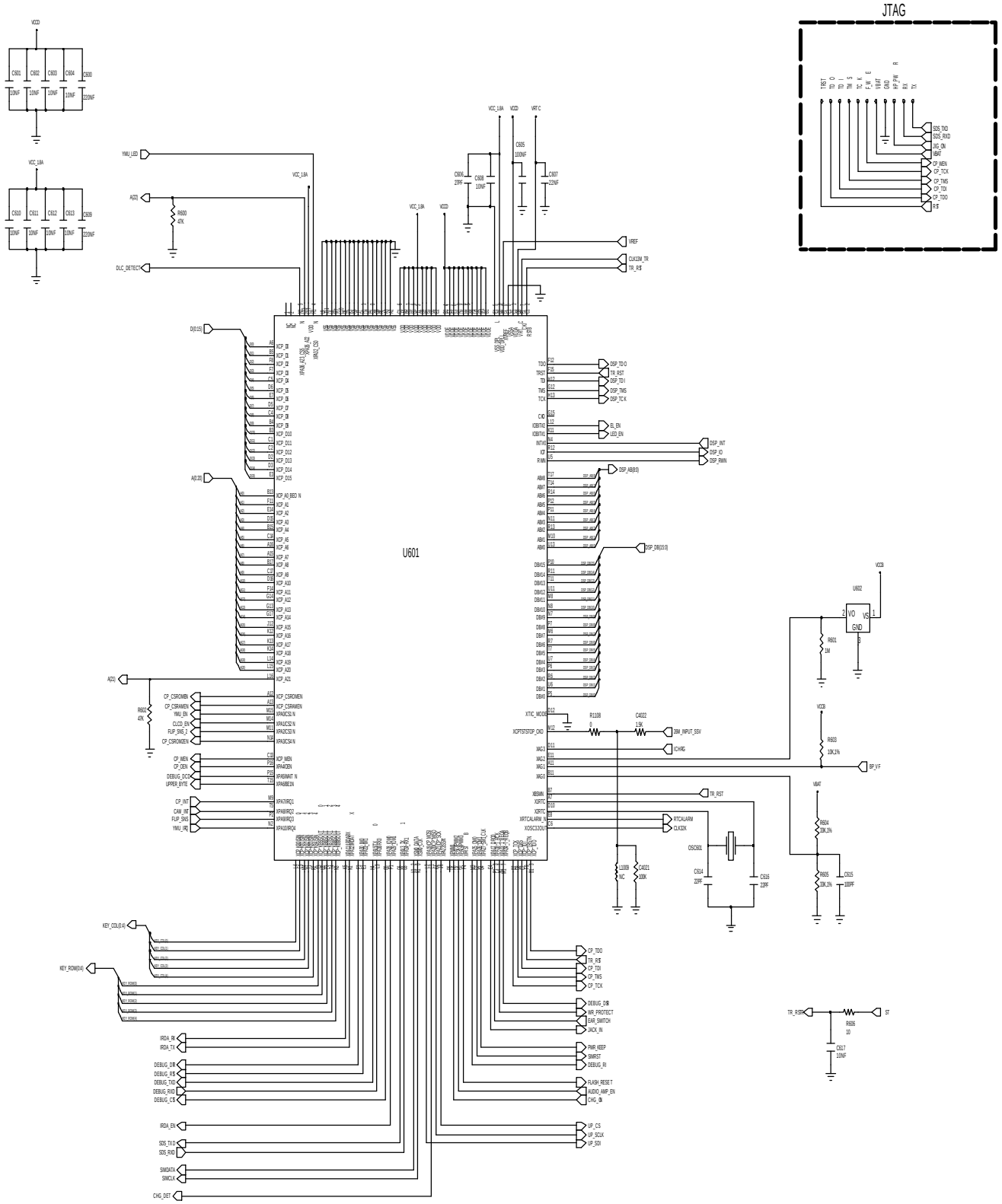

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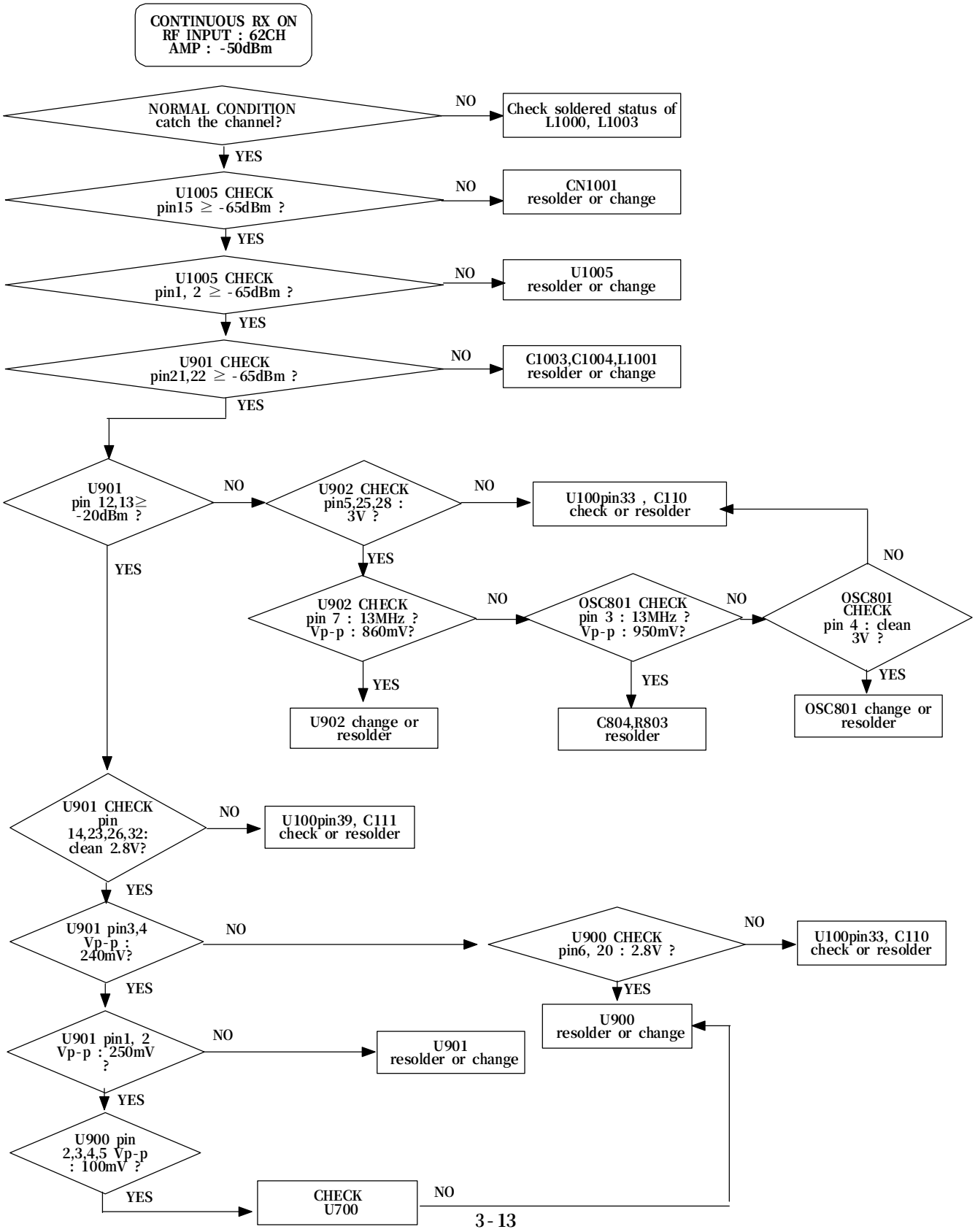
7. EGSM Reciever



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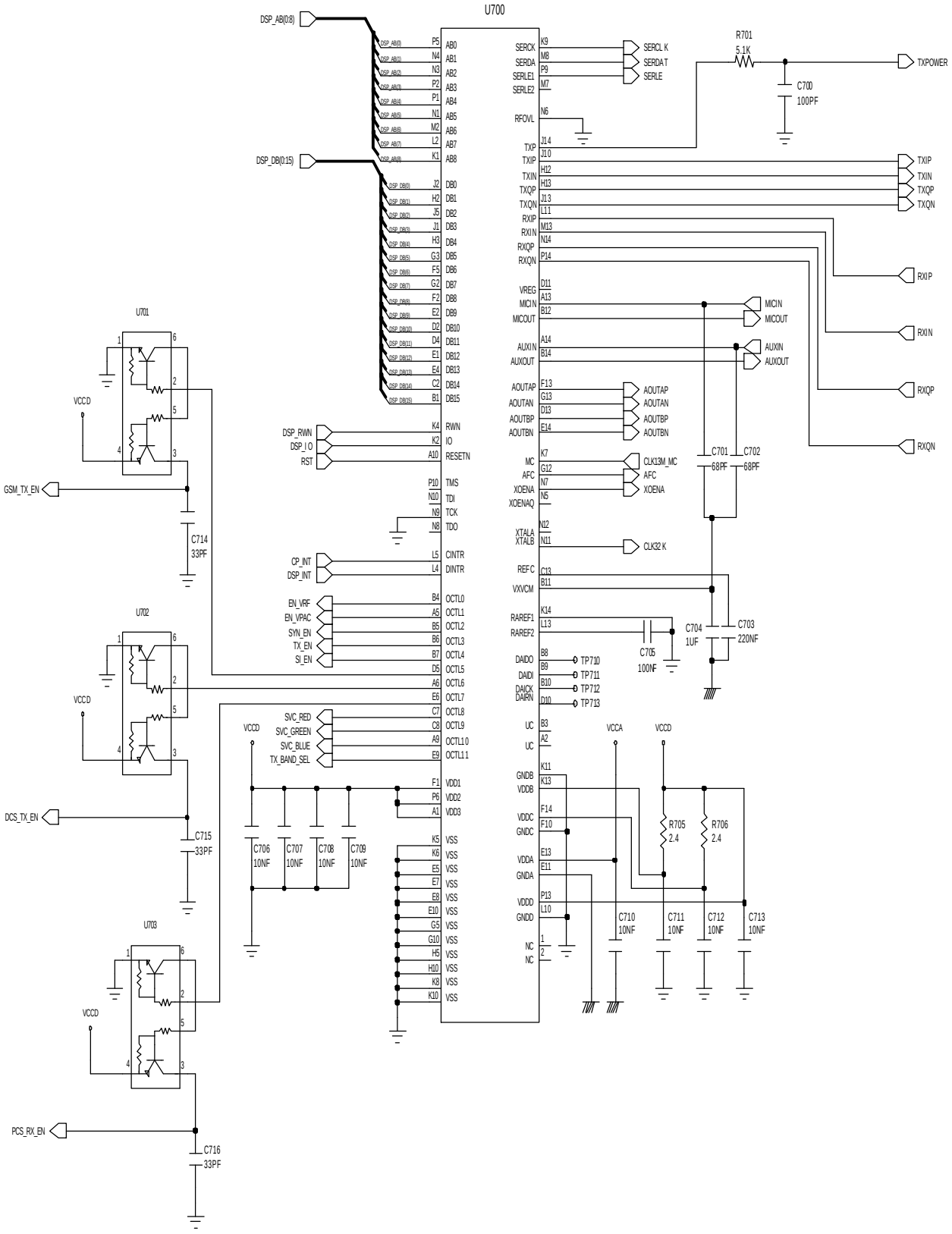

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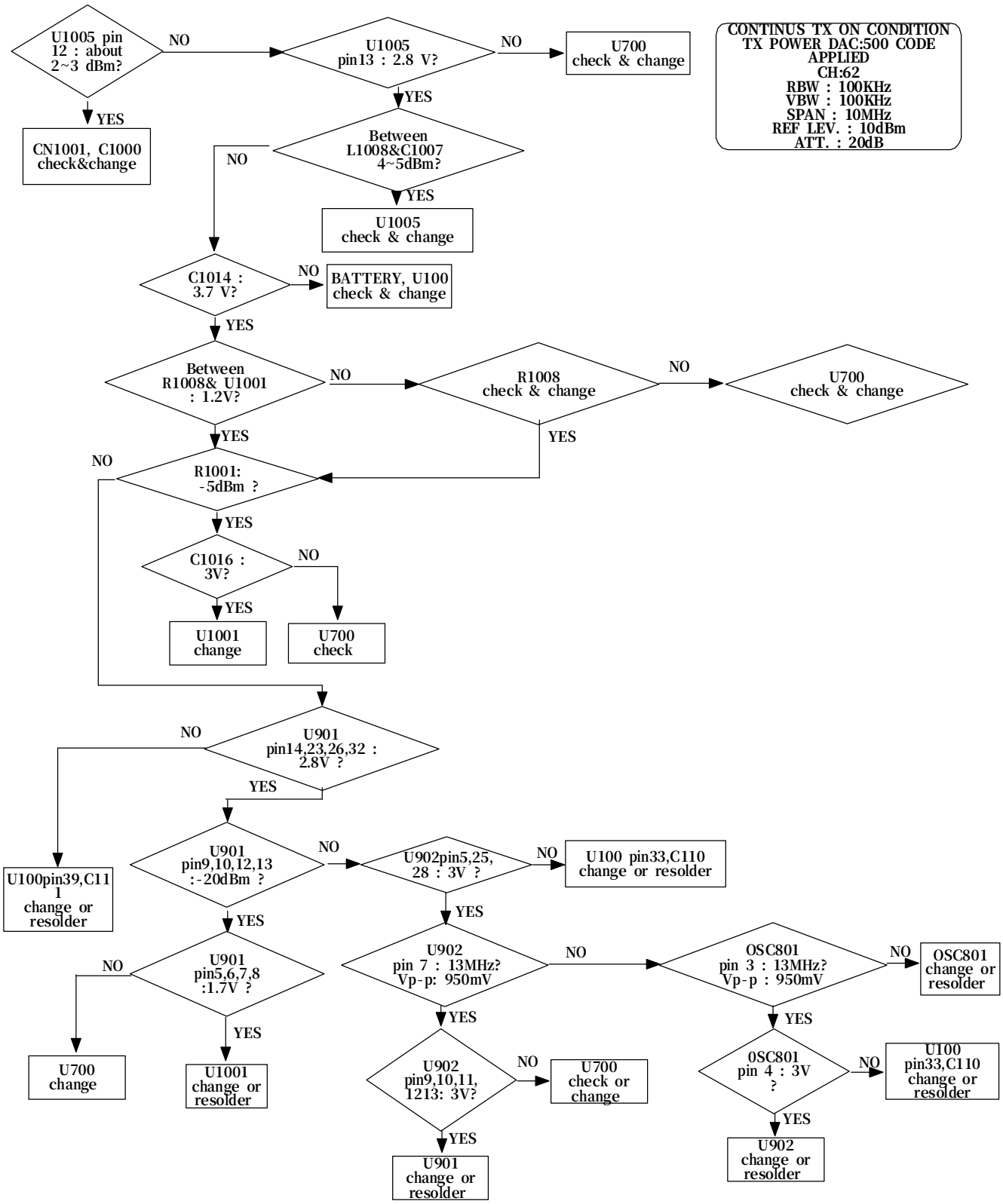
8. EGSM transmitter



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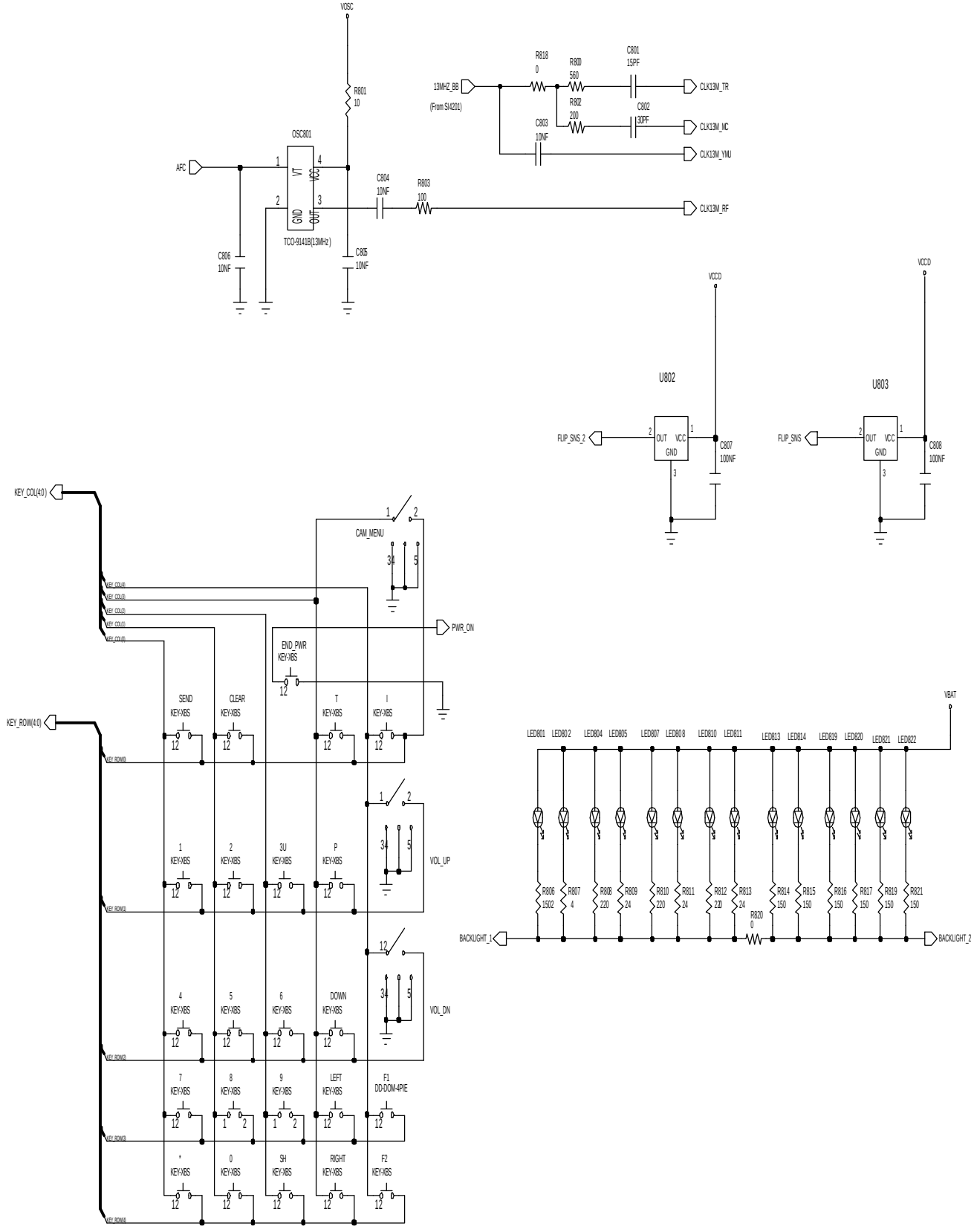

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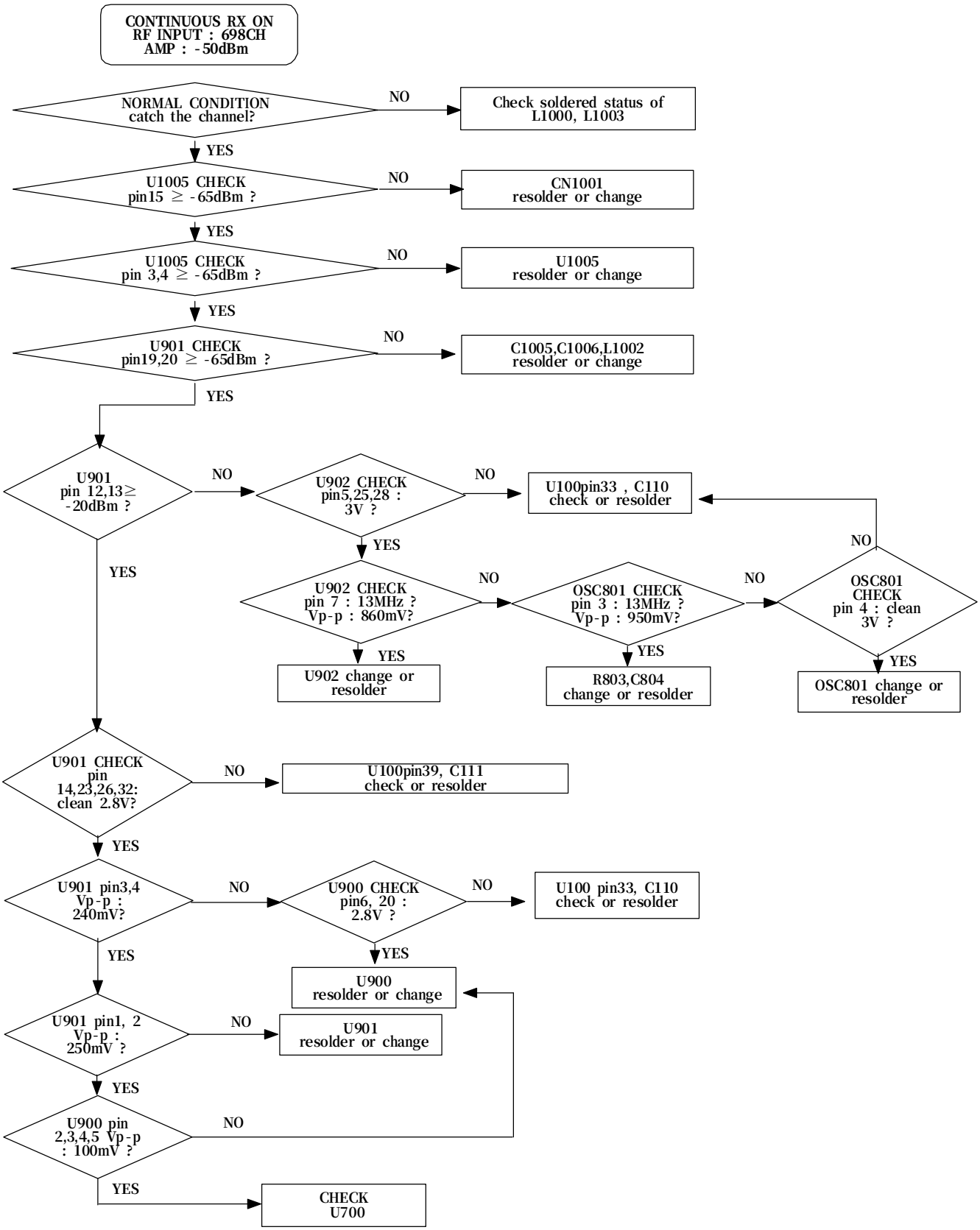
9. DCS Reciever



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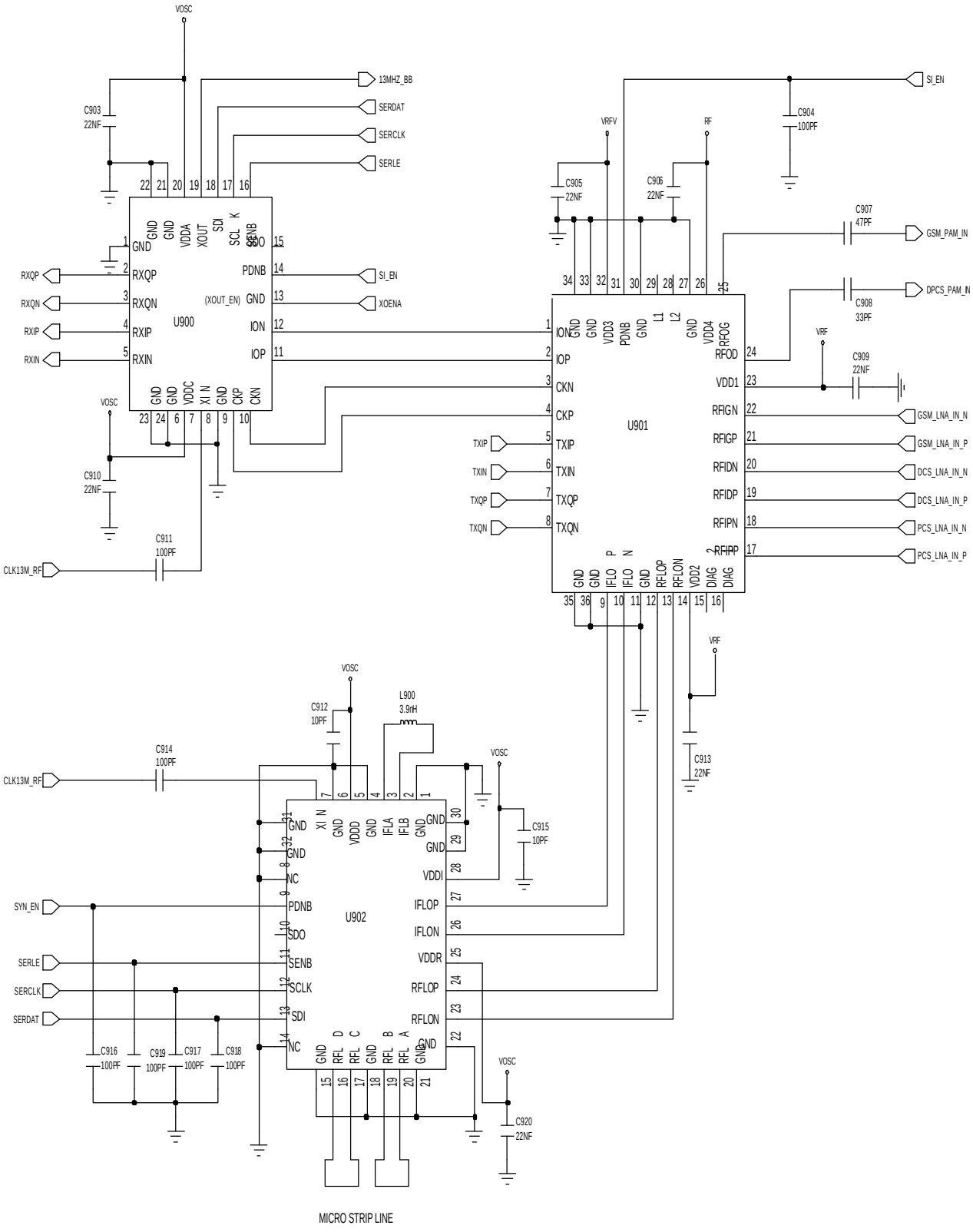

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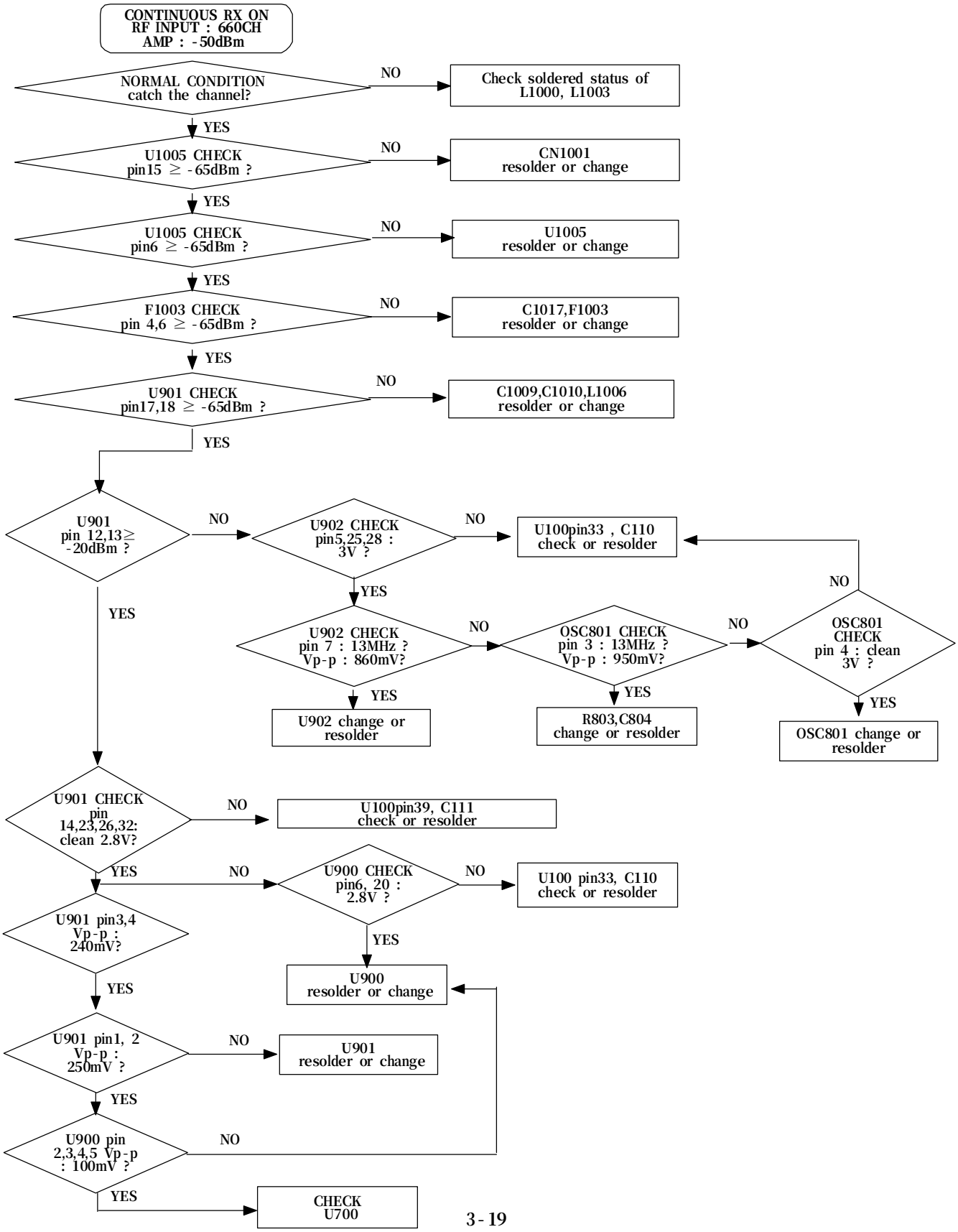
10. PCS Reciever



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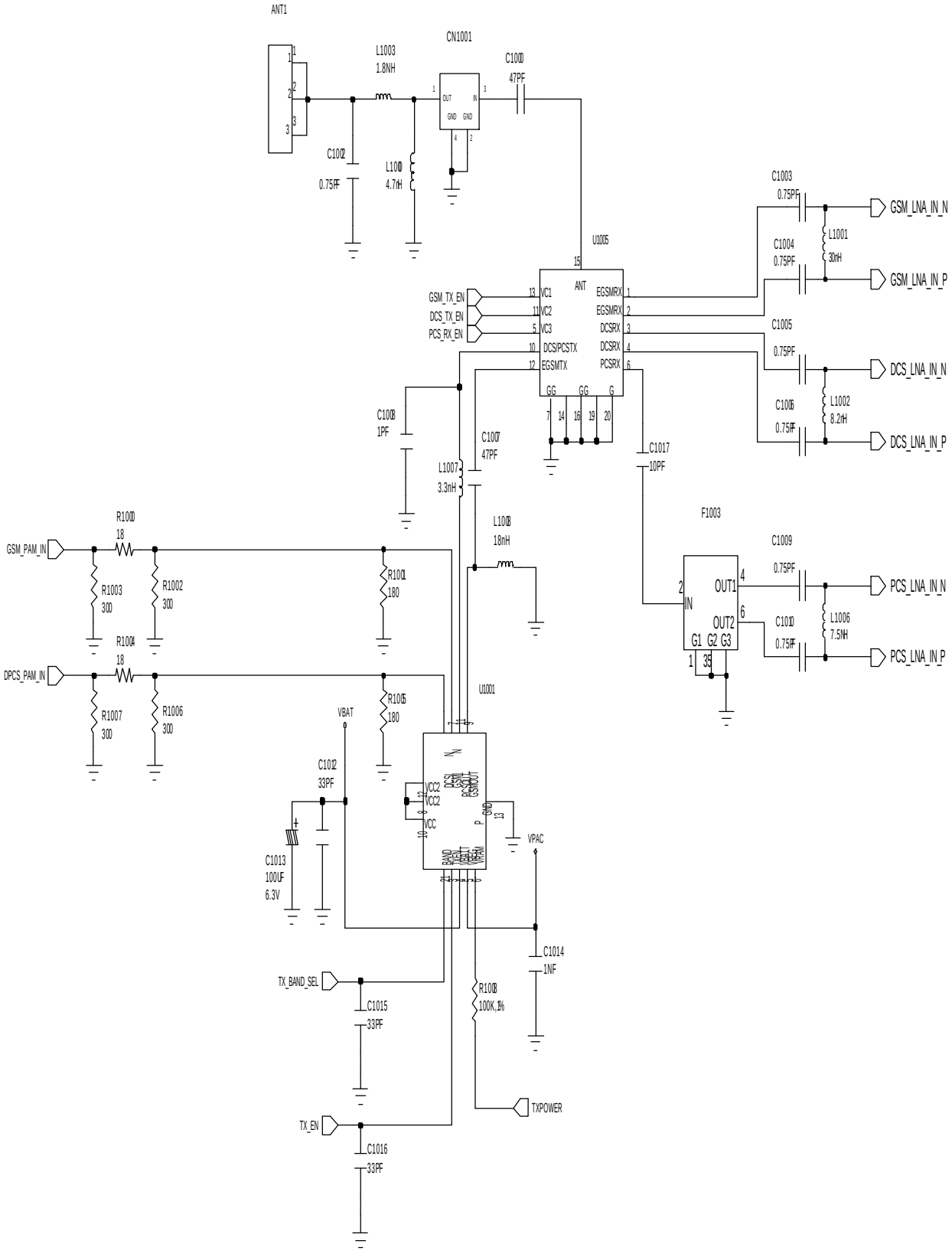

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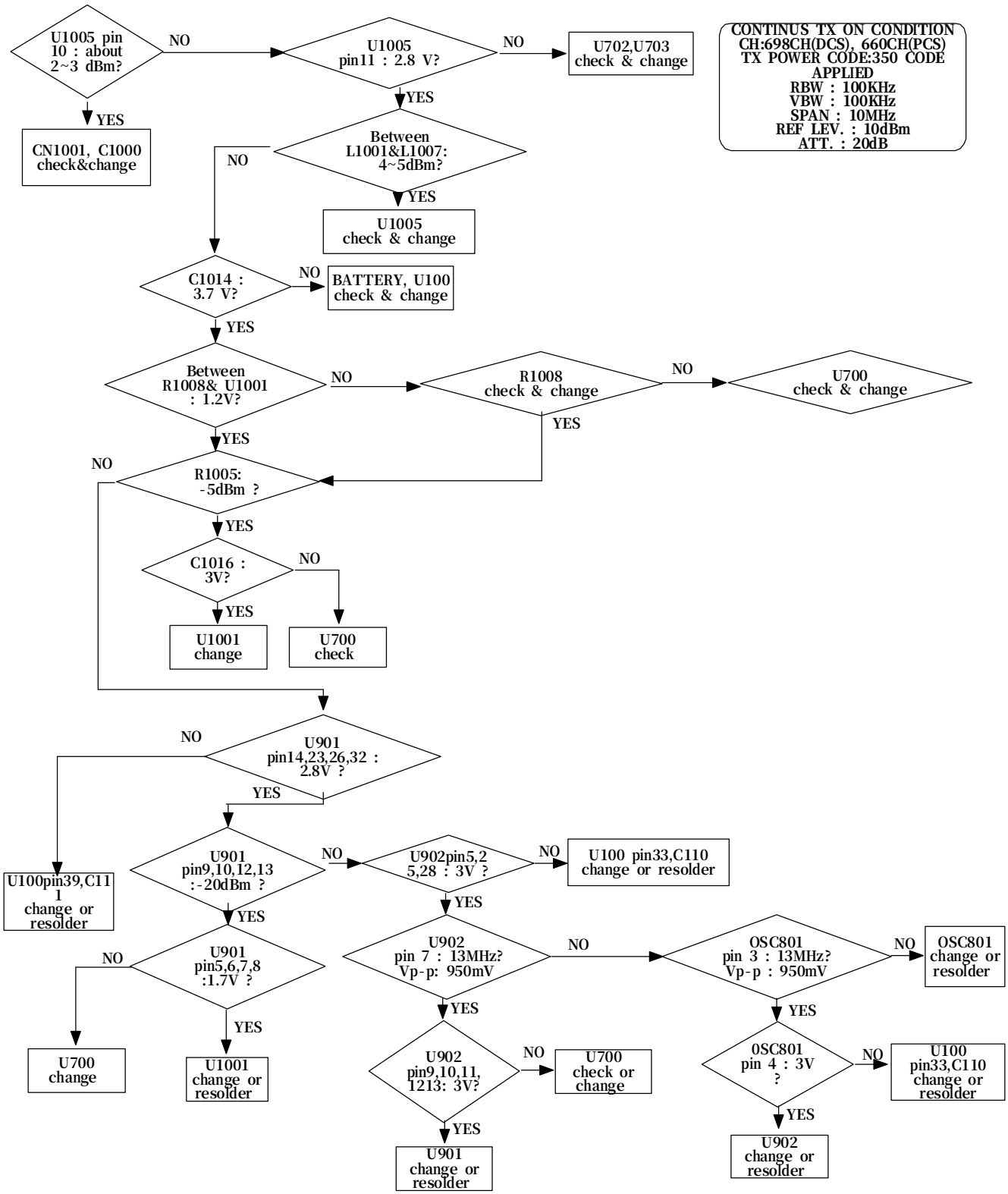
11. DPCS transmitter



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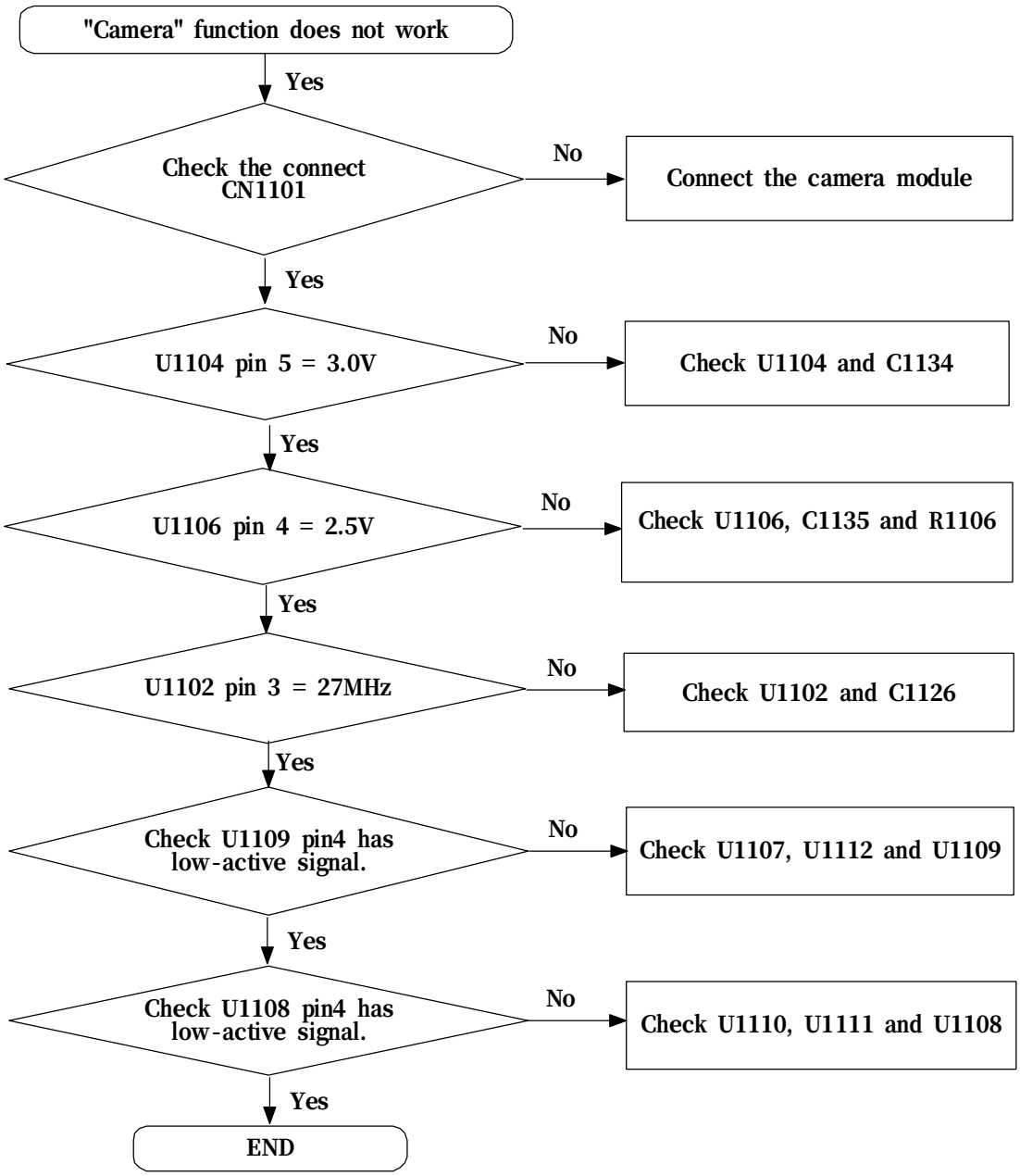
12. Camera part



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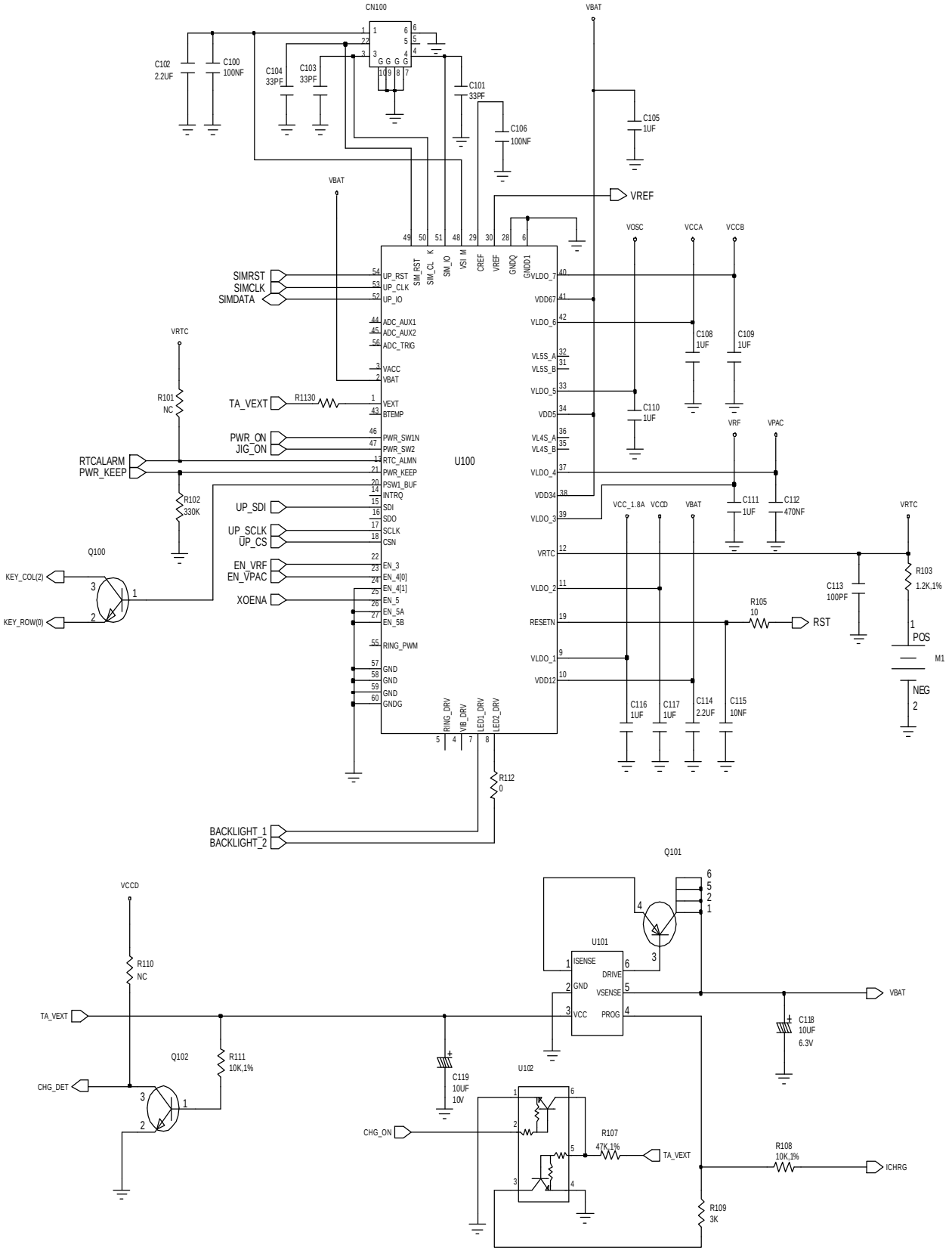

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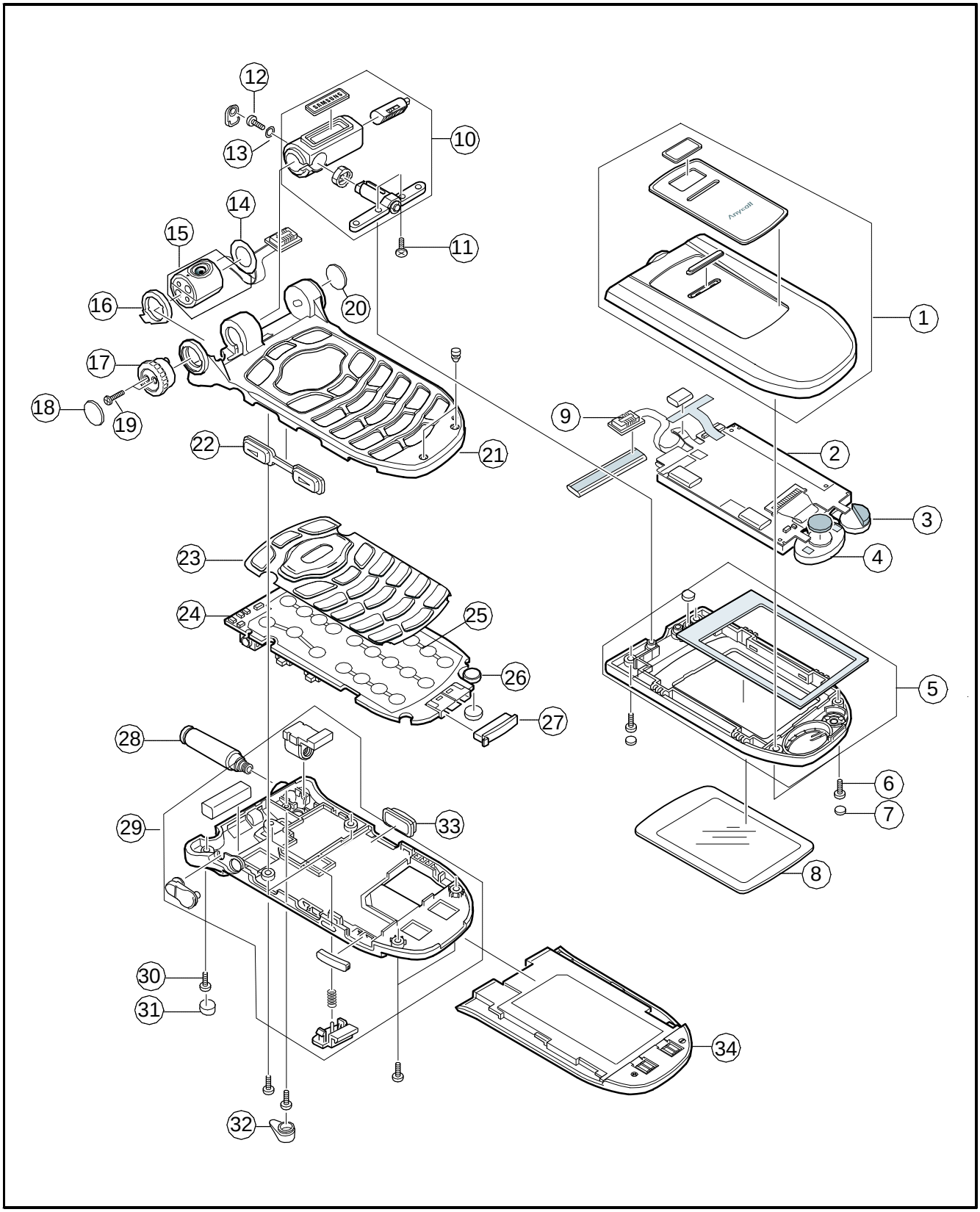
4. SGH-P400 Exploded View and its Parts list

1. Cellular phone Exploded View



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2. Cellular phone Parts list

Location NO.	Description	SEC CODE	Remark
1	FOLDER UPPER	GH75-03185A	
2	MAIN LCD	GH07-00253A	
3	MOTOR	3101-001295	
4	SPEAKER	3001-001423	
5	FOLDER LOWER	GH75-02834A	
6	SCREW	6001-001479	
7	FOL/SCREW COVER	GH73-01508A	
8	WINDOW LCD	GH72-05737B	
9	FPCB	GH59-00802A	
10	HINGE HOUSING	GH75-02571A	
11	SCREW	6001-001456	
12	SCREW	6001-001834	
13	HINGE WASHER	GH71-01152A	
14	CAMERA RING	GH71-01136A	
15	CAMERA	GH59-00803A	
16	ASS'Y PIECE	GH72-07120A	
17	HINGE HOUSING CAP	GH72-06417A	
18	SIDE COVER	GH71-01577A	
19	SCREW	6001-001670	
20	SIDE CAP	GH71-01577A	
21	FRONT COVER	GH75-02833A	
22	VOLUME KEY	GH75-02838A	
23	KEYPAD	GH75-02836C	
24	MAIN PBA	GH92-01496A	
25	DOME SHEET	GH59-00781A	
26	MIC	GH59-00626A	
27	CONN COVER	GH73-01445A	
28	ANTENNA	GH42-00248A	
29	REAR COVER	GH75-02837A	
30	SCREW	6001-001155	
31	REAR SCREW COVER	GH73-01507A	
32	RF COVER	GH73-01506A	
33	SHOT KEY	GH75-02887A	
34	BATTERY	GH43-00983A	

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3. Test Jig (GH80-00865A)

3-1. RF Test Cable
(GH39-00090A)

3-2. Test Cable
(GH39-00127A)

3-3. Serial Cable

3-4. Power Supply Cable

3-5. DATA CABLE
(GH39-00159A)

3-6. TA
(GH44-00171C)

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5. SGH-P400 MAIN Electrical Parts List

SEC Code	Design LOC
GH71-00434A	ANT1
2203-005061	C100,C1103,C1104
2203-000995	C1000,C1007,C907
2203-002677	C1002,C1003,C1004
2203-002677	C1005,C1006,C1009
2203-005288	C1008
2203-000812	C101,C1012,C1015
2203-002677	C1010
2404-001134	C1013
2203-000438	C1014,C202,C221
2203-000812	C1016,C103,C104,C203
2203-000278	C1017,C912,C915
2203-006201	C102
2203-005065	C105,C1135,C231,C232
2203-005482	C106,C1110,C1111
2203-006053	C108,C109,C110,C111
2203-000254	C1100,C1102,C1105
2203-005496	C1101,C301,C600,C609
2404-001100	C1106,C1107,C1134
2203-000254	C1108,C1123,C1126
2203-005061	C1109,C1113,C1114
2203-005482	C1112,C1115,C200
2203-005481	C1116
2203-005061	C1117,C1118,C1119
2203-002494	C112
2203-005061	C1120,C1121,C1122
2203-005061	C1124,C1125,C300
2203-000254	C1127,C1128,C1129
2203-000233	C113,C233,C234,C235
2203-000254	C1130,C1131,C1132
2203-000254	C1133,C115,C205,C504
2203-005796	C114
2203-006053	C116,C117
2404-001105	C118
2404-001268	C119
2203-005509	C201
2203-000812	C204,C206,C207,C208

SEC Code	Design LOC
2203-000812	C209,C210,C211,C212
2203-000812	C213,C214,C215,C216
2203-000812	C217,C218,C219,C220
2203-000812	C222,C223,C224,C225
2203-000812	C226,C227,C228,C229
2203-000812	C230,C411,C714,C715
2203-000233	C236,C237,C238,C239
2203-000233	C240,C241,C615,C700
2203-005061	C400,C402,C408,C414
2203-000311	C401
2203-000438	C4018,C4019,C413
2203-000359	C4020,C419
2007-000162	C4021,R400
2007-000242	C4022
2203-001405	C403,C607,C903,C905
2404-001086	C404,C412
2203-000585	C407
2203-005065	C409,C417,C704
2404-001151	C416
2203-001259	C420
2203-000885	C421
2203-005061	C500,C501,C502,C503
2203-000254	C601,C602,C603,C604
2203-005061	C605,C705
2203-000679	C606
2203-000254	C608,C610,C611,C612
2203-000254	C613,C617,C706,C707
2203-000628	C614,C616
2203-001153	C701,C702
2203-005496	C703
2203-000254	C708,C709,C710,C711
2203-000254	C712,C713,C803,C804
2203-000812	C716,C908
2203-000386	C801
2203-001412	C802
2203-000254	C805,C806
2203-005482	C807,C808

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SEC Code	Design LOC
2203-000233	C904,C911,C914,C916
2203-001405	C906,C909,C910,C913
2203-000233	C917,C918,C919
2203-001405	C920
3404-001152	CAM_MENU,VOL_DN
3709-001244	CN100
3705-001226	CN1001
3711-005079	CN1101
3711-005078	CN200
3710-001673	CN300
3722-001715	CN401
0404-001172	D1101,D1102,D1103
2904-001410	F1003
2703-001747	L1000
2703-002542	L1001
2703-002544	L1002
2703-001729	L1003
2703-002543	L1006
2703-002207	L1007
2703-001722	L1008
2703-001751	L900
0604-001146	LED200
0601-001547	LED801,LED802,LED804
0601-001547	LED805,LED807,LED808
0601-001547	LED810,LED811,LED813
0601-001547	LED814,LED819,LED820
0601-001547	LED821,LED822
4302-001130	M1
2801-004025	OSC601
2809-001260	OSC801
0504-000168	Q100,Q102
0502-001201	Q101
0501-000225	Q400
2007-001288	R1000,R1004
2007-001307	R1001,R1005
2007-007008	R1002,R1003,R1006
2007-007008	R1007

SEC Code	Design LOC
2007-007107	R1008
2007-000758	R102
2007-007137	R103
2007-000172	R105,R200,R502,R606
2007-007139	R107
2007-007142	R108,R111,R603
2007-001323	R109
2007-000982	R1101
2007-000163	R1102,R403
2007-000170	R1103,R601
2007-000148	R1104,R407,R413,R420
2007-001301	R1105
2007-000171	R1107,R1108,R112
2007-000171	R113,R205,R414,R818
2007-000157	R300,R301,R600,R602
2007-000140	R302,R303,R304,R305
2007-000140	R306,R308,R419
2007-000566	R307
2007-003001	R401,R402
2007-000161	R404
2007-000775	R405
2007-001325	R408
2007-000159	R409,R415,R421
2007-000141	R410,R412
2007-001119	R411
2007-001333	R418
2007-000160	R501
2007-007308	R604,R605
2007-000144	R701
2007-007200	R705,R706
2007-002797	R800
2007-000172	R801
2007-001308	R802
2007-000138	R803
2007-001306	R806,R814,R815,R816
2007-001290	R807,R809,R811,R813
2007-000139	R808,R810,R812

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SEC Code	Design LOC
2007-001306	R817,R819,R821
2007-000171	R820
1203-002902	U100
1201-001889	U1001
2909-001191	U1005
1203-002127	U101
0506-001052	U102
GH13-00018A	U1101
2804-001492	U1102
1204-001982	U1103
1203-001720	U1104
1203-002704	U1106
1001-001183	U400
1204-001960	U401
1109-001274	U500
GH09-00025A	U601
1209-001219	U602
1204-001984	U700
0504-001042	U701,U702,U703
1009-001010	U802,U803
1205-002185	U900
1205-002268	U901
1209-001434	U902
3404-001152	VOL_UP
0406-001083	ZD300,ZD301
0403-001427	ZD302
1405-001082	ZD303,ZD304,ZD305
1405-001082	ZD306,ZD307,ZD401
1405-001018	ZD308
1405-001082	ZD402,ZD403,ZD405

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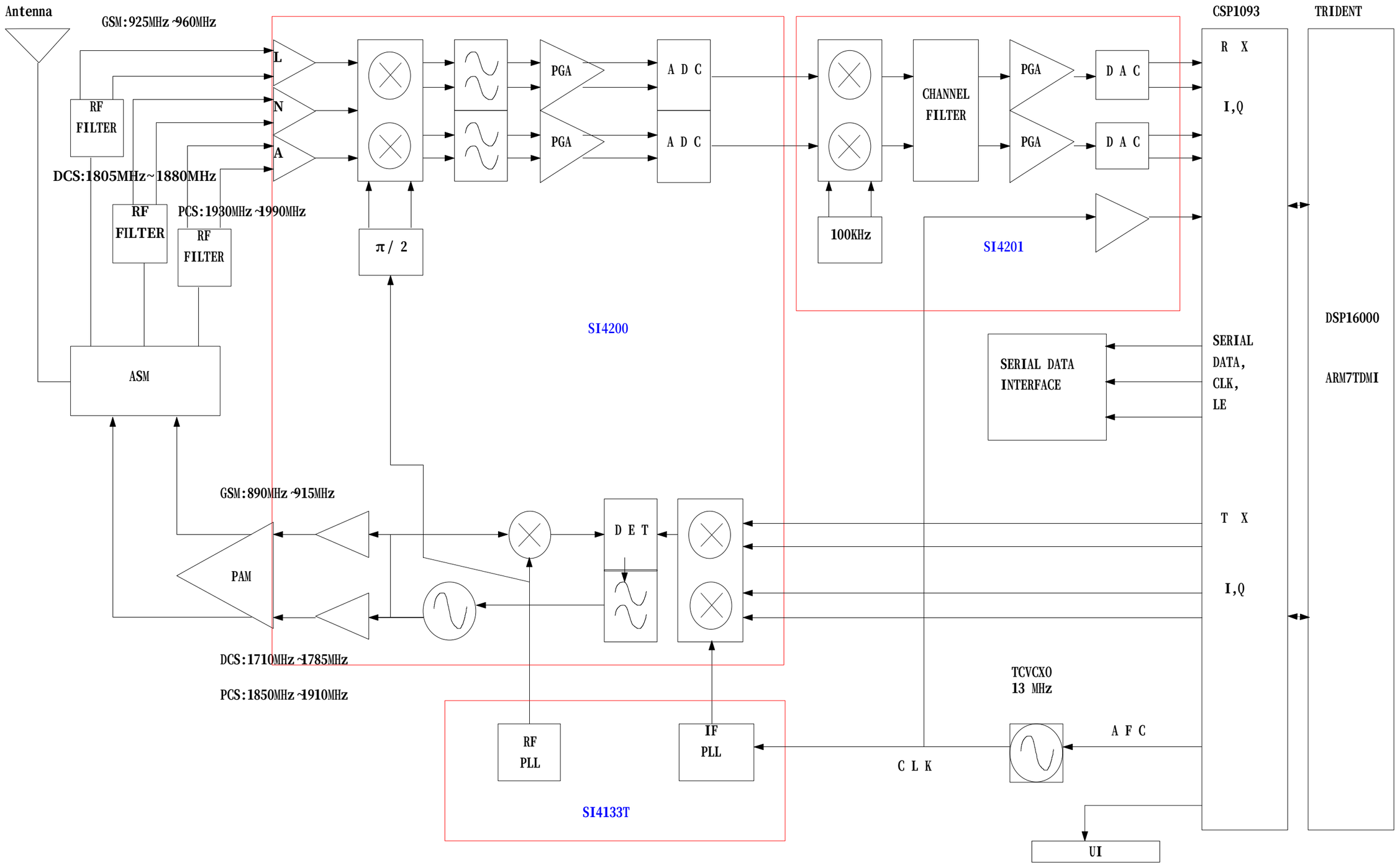
6. SGH-P400 Block Diagrams

1. RF Solution Block Diagram



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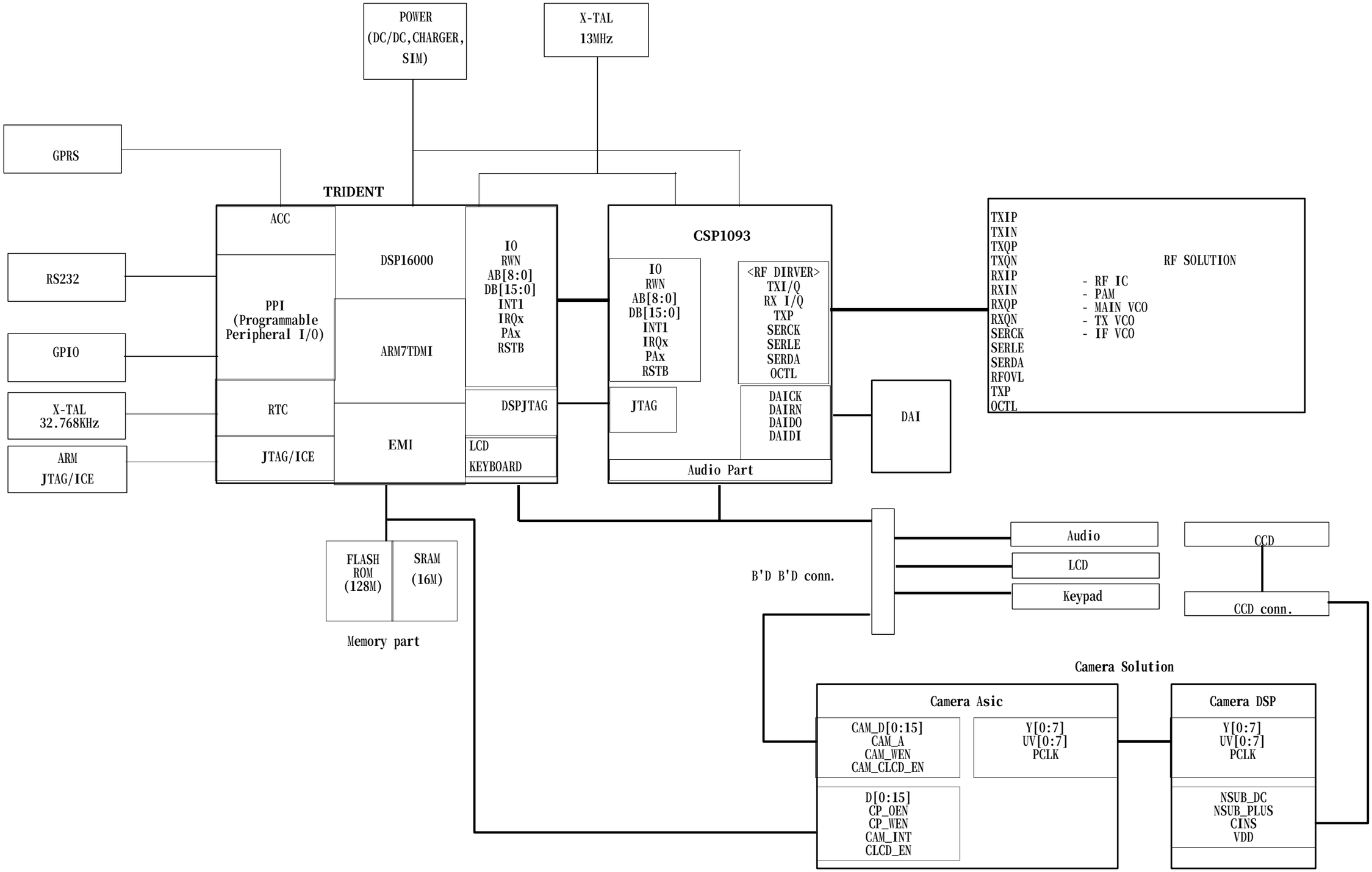
2. Base Band Solution Block Diagram



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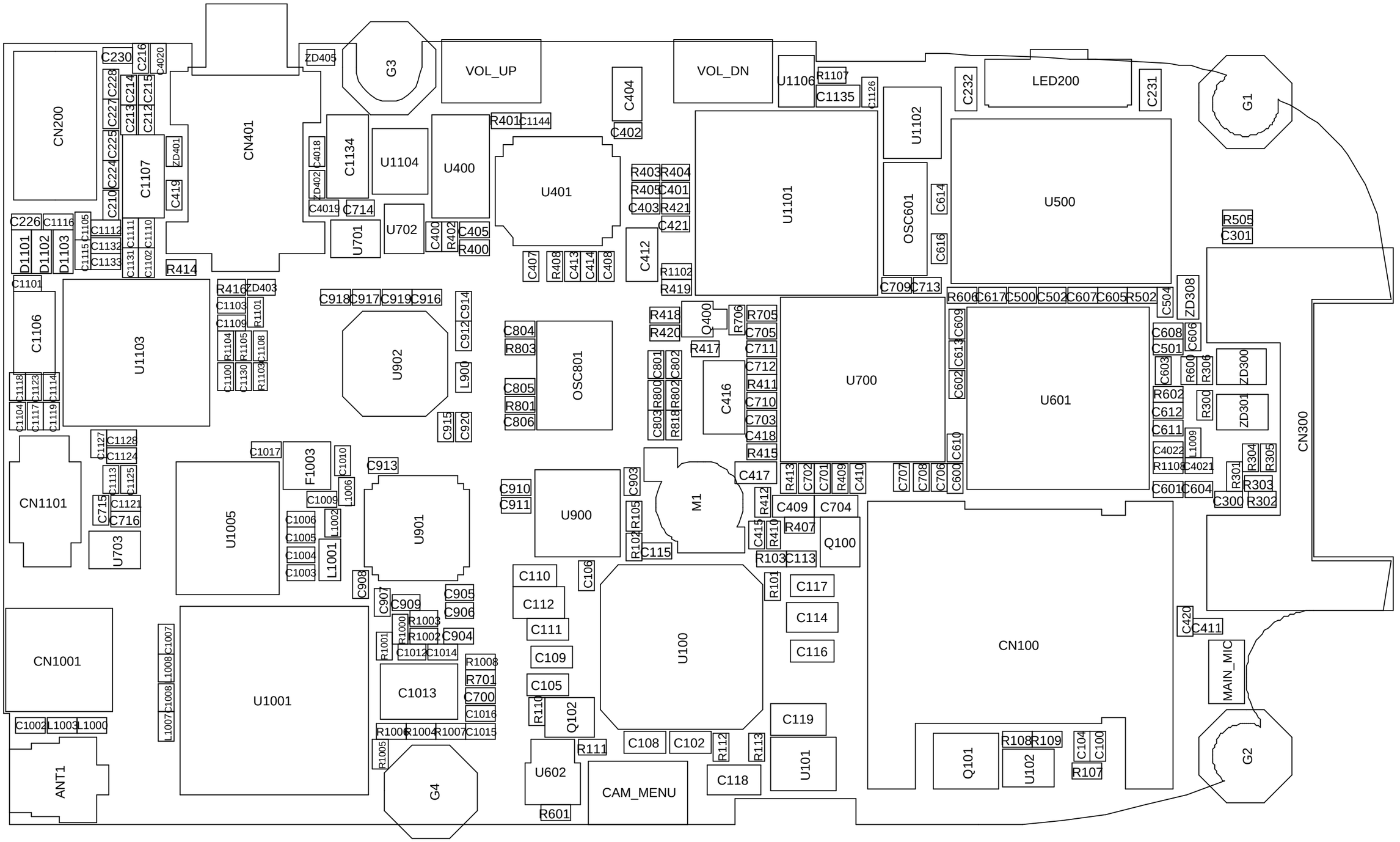
7. SGH-P400 PCB Diagrams

1. Main PCB Top Diagram



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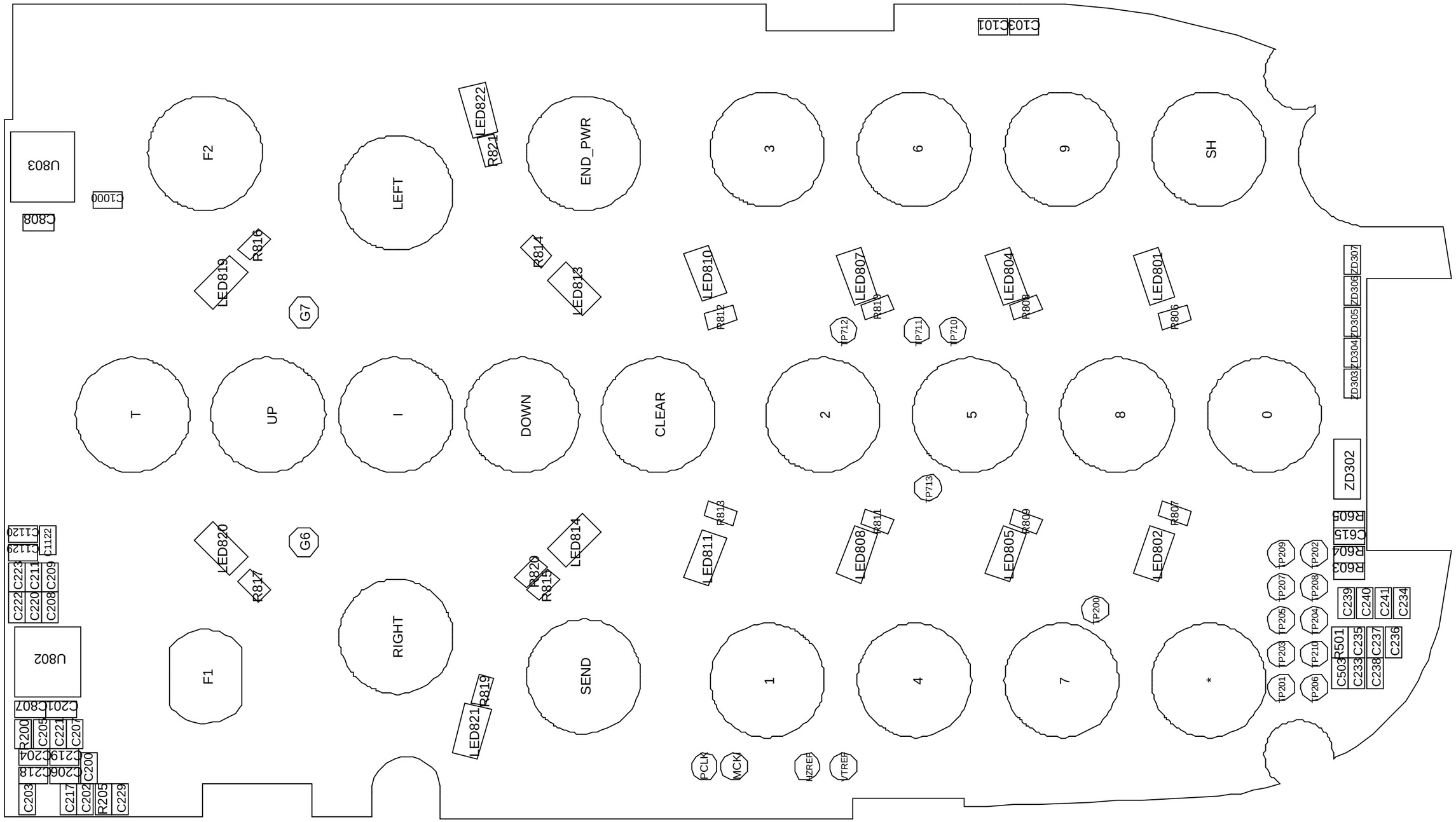
2. Main PCB Bottom Diagram



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