

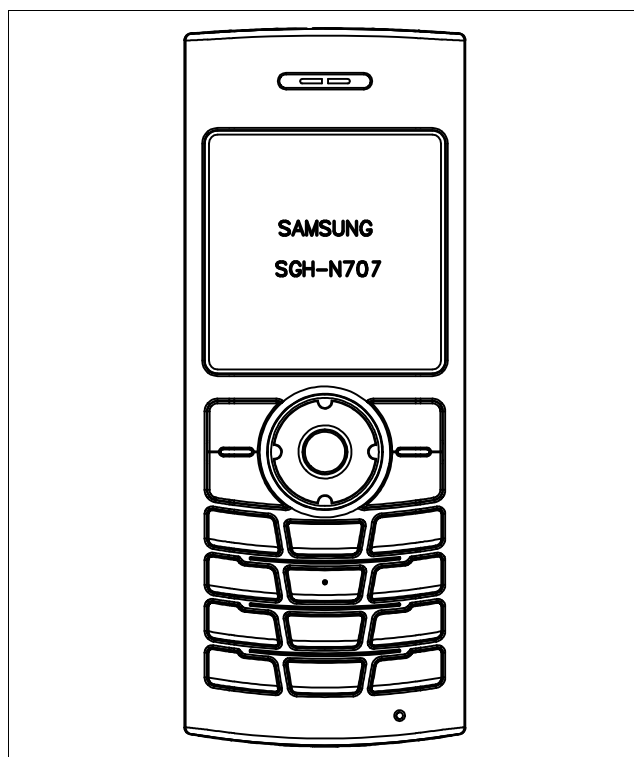
SAMSUNG

GSM TELEPHONE
SGH-N707

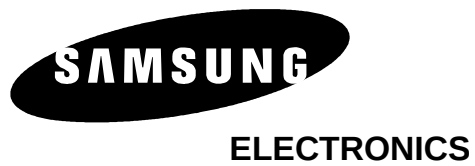
SERVICE *Manual*

GSM TELEPHONE

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Samsung Electronics Co.,Ltd. APRIL. 2004
Printed in Korea.

Code No.: GH68-05461A
BASIC.

1. SGH-N707 Specification

1. GSM General Specification

	GSM850	PCS1900
Freq. Band[MHz] Uplink/Downlink	824~849 869~894	1850~1910 1930~1990
ARFCN range	128~251	512~810
Tx/Rx spacing	45MHz	80MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK
MS Power	33dBm~5dBm	30dBm~0dBm
Power Class	5pcl ~ 19pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm
TDMA Mux	8	8

2. GSM TX power class

TX Power control level	GSM850
5	33 ±2 dBm
6	31 ±2 dBm
7	29 ±2 dBm
8	27 ±2 dBm
9	25 ±2 dBm
10	23 ±2 dBm
11	21 ±2 dBm
12	19 ±2 dBm
13	17 ±2 dBm
14	15 ±2 dBm
15	13 ±2 dBm
16	11 ±3 dBm
17	9 ±3dBm
18	7 ±3 dBm
19	5 ±3 dBm

TX Power control level	PCS1900
0	30 ±2 dBm
1	28 ±3 dBm
2	26 ±3 dBm
3	24 ±3 dBm
4	22 ±3 dBm
5	20 ±3 dBm
6	18 ±3 dBm
7	16 ±3 dBm
8	14 ±3 dBm
9	12 ±4 dBm
10	10 ±4 dBm
11	8 ±4dBm
12	6 ±4 dBm
13	4 ±4 dBm
14	2 ±5 dBm
15	0 ±5 dBm

2. SGH-N707 Circuit Description

1. SGH-N707 RF Circuit Description

1) RX PART

1. FEM(U402(SWITCHPLEXER+FILTER)) → Switching Tx, Rx path for GSM850, and PCS1900 by logic controlling.
2. FEM Control Logic (U402) → Truth Table

	VC1	VC2
DCS / PCS Tx Mode	L	H
GSM Tx Mode	H	L
GSM / PCS Rx Mode	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (U402(SWITCHPLEXER+FILTER)) → For filtering the frequency band between 869 ~ 894 MHz
- PCS FILTER(U402(SWITCHPLEXER+FILTER)) → For filtering the frequency band 1930 and 1990 MHz.

4. VC-TCXO (OSC401)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U101 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. SI 4205 (U404)

This chip integrates two differential-input LNAs.

The GSM input supports the GSM850, PCS input supports the DCS1900. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from frequency synthesizer. The RFLO frequency is between 1737.8 ~ 1989.9 MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

Also, this chip down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals.

After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U404 chip.

SI4205 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U403).

The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		PCS	-65dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		PCS	-68dBc

2. Baseband Circuit description of SGH-N707

1) CSP2200B1

1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable LDO provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as two LED drivers and two call-alert drivers, aid in reducing both board area and system complexity. A four-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the CSP2200B1 and enables system designers to maximize both standby and talk times. Error reporting is provided via an interrupt signal and status register. Supervisory functions, including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

2. Battery Charge Management

A battery charge management block, incorporating an internal PMOS switch, and an 8-bit ADC, provides fast, efficient charging of single-cell Li-Ion battery. Used in conjunction with a current-limited voltage source, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard illumination. LED1_DRV is controlled via LED1_[0:2] and can be programmed to sink from 15mA to 60mA in 7.5mA steps. LED2_DRV is controlled via LED2_[0:2] and can be programmed to sink from 5mA to 40mA in 5mA steps.

Both LED drivers are capable of sinking their maximum output current at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

4. Vibrator Motor Driver

The vibrator motor driver is a independent voltage regulator to drive a small dc motor that silently alerts the user of an incoming call. The driver is a 3.0V constant source while sinking up to 180mA and controlled by enable signal of main chip. For efficient use and safety, the vibrator motor should be connected between the regulator output and the ground.

2) LCD

LCD is consisted of main LCD(B/W STN LCD). Chip select signals of EMI part in the trident, LCD_CS, can enable main LCD. VDD_EL signal enables EL of main LCD. In sleep mode, EL are turned off.

These two signals are from IO part of the DSP in the trident. RST signal from CSP2200B1 initiates the initial process of the LCD.

16-bit data lines(D(0)~D(15)) transfers data and commands to LCD . Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data.

The signals which inform the input or output state to LCD, are required. But this system is not necessary for read enable signal. CP_WEN signal is only used to write data or commands to LCD.

Power signal for operating LCD driver is VCCD.

3) JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'.

CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

4) Keypad

This is consisted of key interface pins in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix.

So power on/off signal is connected with CSP2200 to enable CSP2200.

5) IF connector

It is 18-pin connector, and separated into two parts. One is a power supply part for main system. And the other is designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, TA, VF, and GND. They connected to power supply IC, microprocessor and signal processor IC.

6) Audio

AOUTAP, AOUTAN from CSP2200 is connected to the speaker via analog switch. MICIN and MICOUT are connected to the main MIC.

YMU759 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decoder that are included in this device.

As a synthesis, YMU759 is equipped 16 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU759 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU759 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibrator and a circuit for controlling LEDs synchronous with music.

7) Memory

This system uses AMD's memory, S71JL064HA0BAW110.

It is consisted of 64M bits flash memory and 16M bits PSRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP2200. It has 22 bit address lines, A[0~21]. They are also connected. CP_CSROMEN signal, chip select signal in the trident, enable flash memories. They use 2.8 volt supply voltage, VCCD.

During wrting process, CP_WEN is low and it enables writing process to flash memory and PSRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or PSRAM to data lines. Each chip select signals in the trident select flash memory or PSRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use RST. A[0] signal enables lower byte of PSRAM and UPPER_BYTE signal enables higher byte of PSRAM.

8) Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACCs(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface. DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP2200. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU762.

ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.

CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.

Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communications using data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).

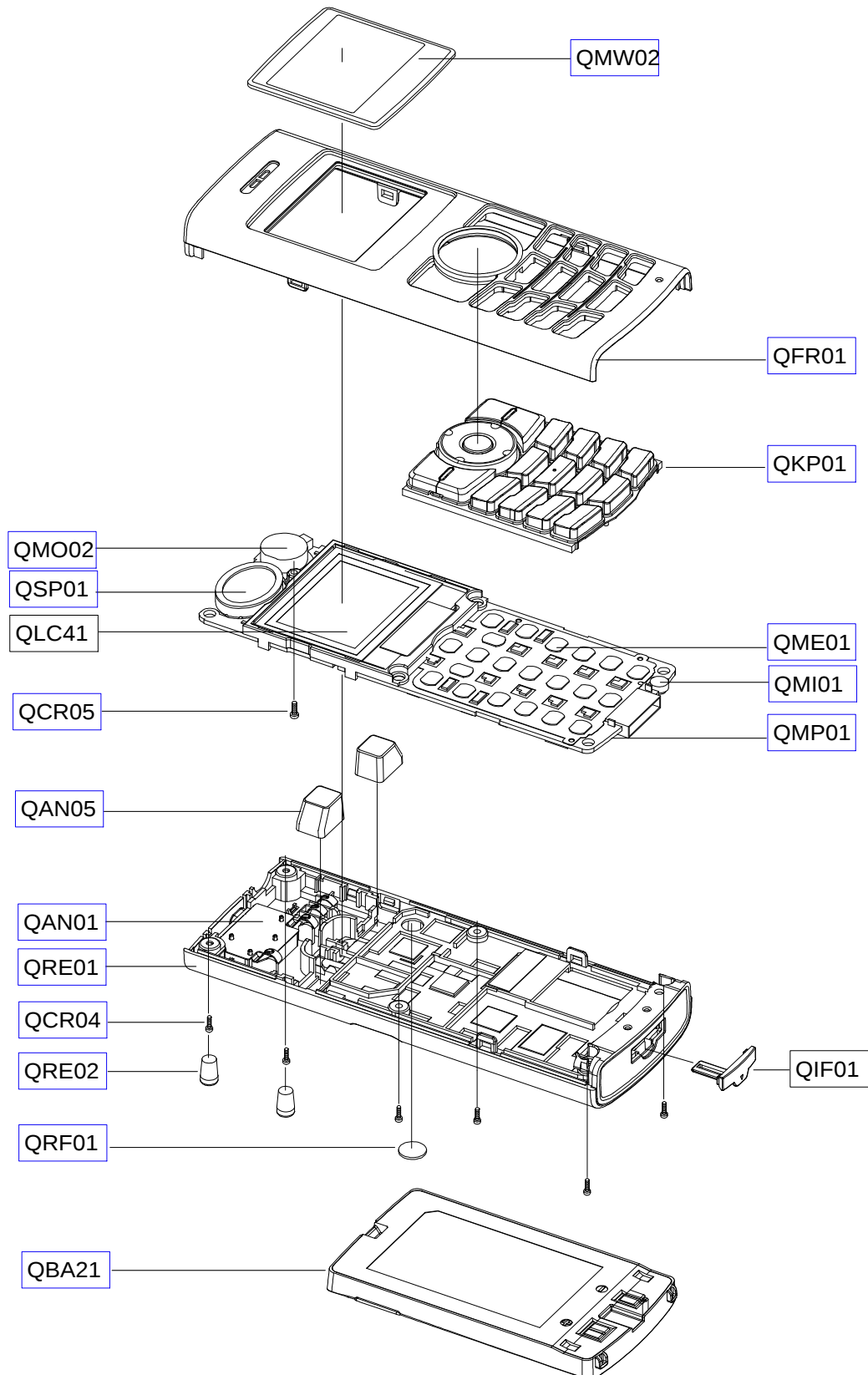
And UP_CS/SCLK/SDI, control signals for CSP2200 are outputted through PPI pins. It has signal port for charging(CHG_DET), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Converter) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD with DSP IP pins.

9) X-TAL(13MHz)

This system uses the 13MHz TCXO. AFC control signal from CSP1093 controls frequency from 13MHz x-tal. . This clock is fed to CSP1093,Trident,YMU759 and Silab solution.

3. SGH-N707 Exploded View and its Parts list

1. Cellular phone Exploded View - 1



2. Cellular phone Parts list

Location NO.		Description	SEC CODE	Remark
QMW02		PMO-MAIN WINDOW	GH72-13316A	
QFR01		MEC-FRONT COVER	GH75-04537A	
QIF01		PMO-IF COVER	GH72-16745A	
QKP01		MEC-KEYPAD ASSY	GH75-04539A	
QSP01		SPEAKER	3001-001576	
QMO02		MOTOR	3101-001328	
QMP01		MIAN PBA	GH92-01773A	
QLC41		LCD	GH07-00548A	
QME01		UNIT METAL DOME	GH59-01456A	
QMI01		MICROPHONE ASSY	GH30-00125A	
QCR05		SCREW	6001-001478	
QAN05		MEC-INTENA RUBBER	GH75-05620A	
QRE01		REAR COVER	GH75-04538A	
QCR04		SCREW-MACHINE	6001-001479	
QRE02		PMO-REAR BUMPER	GH72-16829A	
QRF01		MPR-R/F COVER	GH74-08243A	
QBA21		BATTERY-820MAH	GH43-01358A	
QAN01		ANTENNA	GH42-00429A	

3. Test Jig (GH80-00865A)



3-1. RF Test Cable
(GH39-00182A)



3-2. Test Cable
(GH39-00127A)



3-3. Serial Cable



3-4. Power Supply Cable



3-5. DATA CABLE
(GH39-00143B)



3-6. TA
(GH44-00284A)



4. SGH-N707 MAIN Electrical Parts List

SEC CODE	Design LOC
0403-001387	ZD629
0403-001427	ZD628
0403-001511	ZD301
0404-001172	D501
0406-001150	ZD501
0406-001150	ZD502
0501-000481	Q301
0504-001113	Q102
0601-001094	LED601
0601-001094	LED602
0601-001094	LED605
0601-001094	LED606
0601-001094	LED607
0601-001094	LED608
0601-001094	LED631
0601-001094	LED632
0601-001094	LED633
0601-001094	LED634
0601-001094	LED635
0601-001094	LED636
0601-001956	LED610
0801-000796	U102
1001-001261	U501
1003-001395	U302
1109-001309	U202
1201-002177	U403
1203-001917	U601
1203-003109	U107
1203-003304	U101
1204-001811	U502
1205-002433	U404
1209-001219	U203
1405-001082	ZD601
1405-001082	ZD602
1405-001082	ZD603
1405-001082	ZD604
1405-001082	ZD605
1405-001082	ZD606
1405-001082	ZD607

SEC CODE	Design LOC
1405-001082	ZD608
1405-001082	ZD609
1405-001082	ZD610
1405-001082	ZD611
1405-001082	ZD612
1405-001082	ZD613
1405-001082	ZD614
1405-001082	ZD615
1405-001082	ZD616
1405-001082	ZD617
1405-001082	ZD618
1405-001082	ZD619
1405-001082	ZD620
1405-001082	ZD621
1405-001082	ZD622
1405-001082	ZD623
1405-001082	ZD624
2007-000138	R103
2007-000138	R113
2007-000138	R424
2007-000140	R515
2007-000140	R516
2007-000140	R617
2007-000140	R618
2007-000140	R619
2007-000140	R620
2007-000140	R621
2007-000140	R622
2007-000140	R623
2007-000140	R624
2007-000140	R625
2007-000140	R627
2007-000140	R628
2007-000140	R629
2007-000141	R420
2007-000148	R109
2007-000148	R110
2007-000148	R202
2007-000148	R214

SEC CODE	Design LOC
2007-000148	R423
2007-000148	R510
2007-000148	R512
2007-000157	R207
2007-000157	R609
2007-000157	R610
2007-000162	R111
2007-000162	R112
2007-000162	R114
2007-000162	R201
2007-000162	R206
2007-000162	R501
2007-000162	R511
2007-000162	R513
2007-000164	R504
2007-000171	R102
2007-000171	R104
2007-000171	R105
2007-000171	R106
2007-000171	R108
2007-000171	R210
2007-000171	R213
2007-000171	R302
2007-000171	R425
2007-000171	R426
2007-000171	R509
2007-000171	R518
2007-000171	R519
2007-000171	R521
2007-000690	R301
2007-000775	R505
2007-000775	R506
2007-001119	R517
2007-001217	R601
2007-001217	R602
2007-001217	R605
2007-001217	R606
2007-001217	R607
2007-001217	R608

SEC CODE	Design LOC
2007-001217	R631
2007-001217	R632
2007-001217	R633
2007-001217	R634
2007-001217	R635
2007-001217	R636
2007-001292	R502
2007-001292	R503
2007-001319	R101
2007-001325	R507
2007-002797	R421
2007-003001	R422
2007-003025	R630
2007-007100	R205
2007-007138	R402
2007-007142	R208
2007-007308	R211
2007-007308	R212
2007-008117	R107
2203-000189	C310
2203-000189	C311
2203-000189	C312
2203-000189	C313
2203-000189	C314
2203-000233	C110
2203-000233	C401
2203-000233	C402
2203-000233	C423
2203-000233	C429
2203-000233	C430
2203-000233	C431
2203-000233	C440
2203-000233	C502
2203-000233	C503
2203-000233	C505
2203-000233	C508
2203-000254	C201
2203-000254	C202
2203-000254	C203

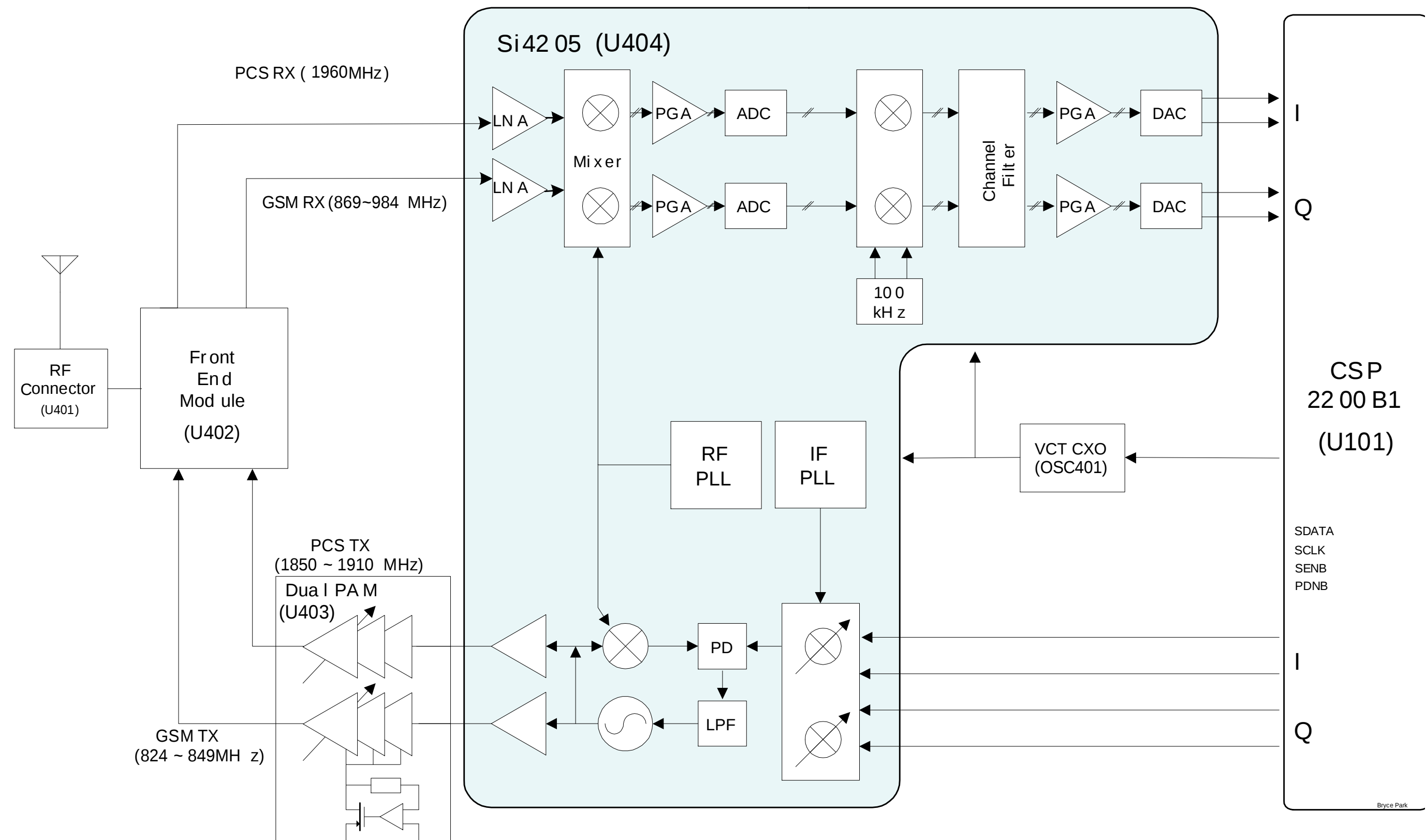
SEC CODE	Design LOC
2203-000254	C204
2203-000254	C205
2203-000254	C206
2203-000254	C207
2203-000254	C208
2203-000254	C212
2203-000254	C418
2203-000254	C419
2203-000254	C438
2203-000254	C441
2203-000254	C442
2203-000254	C443
2203-000254	C449
2203-000278	C530
2203-000425	C439
2203-000438	C512
2203-000628	C220
2203-000628	C221
2203-000628	C407
2203-000628	C410
2203-000628	C435
2203-000654	C504
2203-000679	C211
2203-000812	C107
2203-000812	C108
2203-000812	C109
2203-000812	C436
2203-000885	C303
2203-000995	C414
2203-000995	C434
2203-001072	C101
2203-001072	C102
2203-001072	C114
2203-001072	C215
2203-001072	C216
2203-001405	C507
2203-001598	C111
2203-001598	C112
2203-001598	C116

SEC CODE	Design LOC
2203-001652	C113
2203-005061	C103
2203-005061	C106
2203-005061	C117
2203-005061	C119
2203-005061	C124
2203-005061	C213
2203-005061	C214
2203-005061	C217
2203-005061	C218
2203-005061	C222
2203-005061	C223
2203-005061	C422
2203-005061	C506
2203-005061	C510
2203-005061	C513
2203-005061	C532
2203-005065	C302
2203-005065	C305
2203-005065	C306
2203-005065	C307
2203-005065	C523
2203-005065	C609
2203-005065	C610
2203-005281	C411
2203-005281	C413
2203-005288	C408
2203-005288	C409
2203-005446	C450
2203-005480	C219
2203-005482	C304
2203-005482	C501
2203-005496	C118
2203-005496	C209
2203-005496	C210
2203-005509	C515
2203-005509	C521
2203-006093	C115
2203-006093	C120

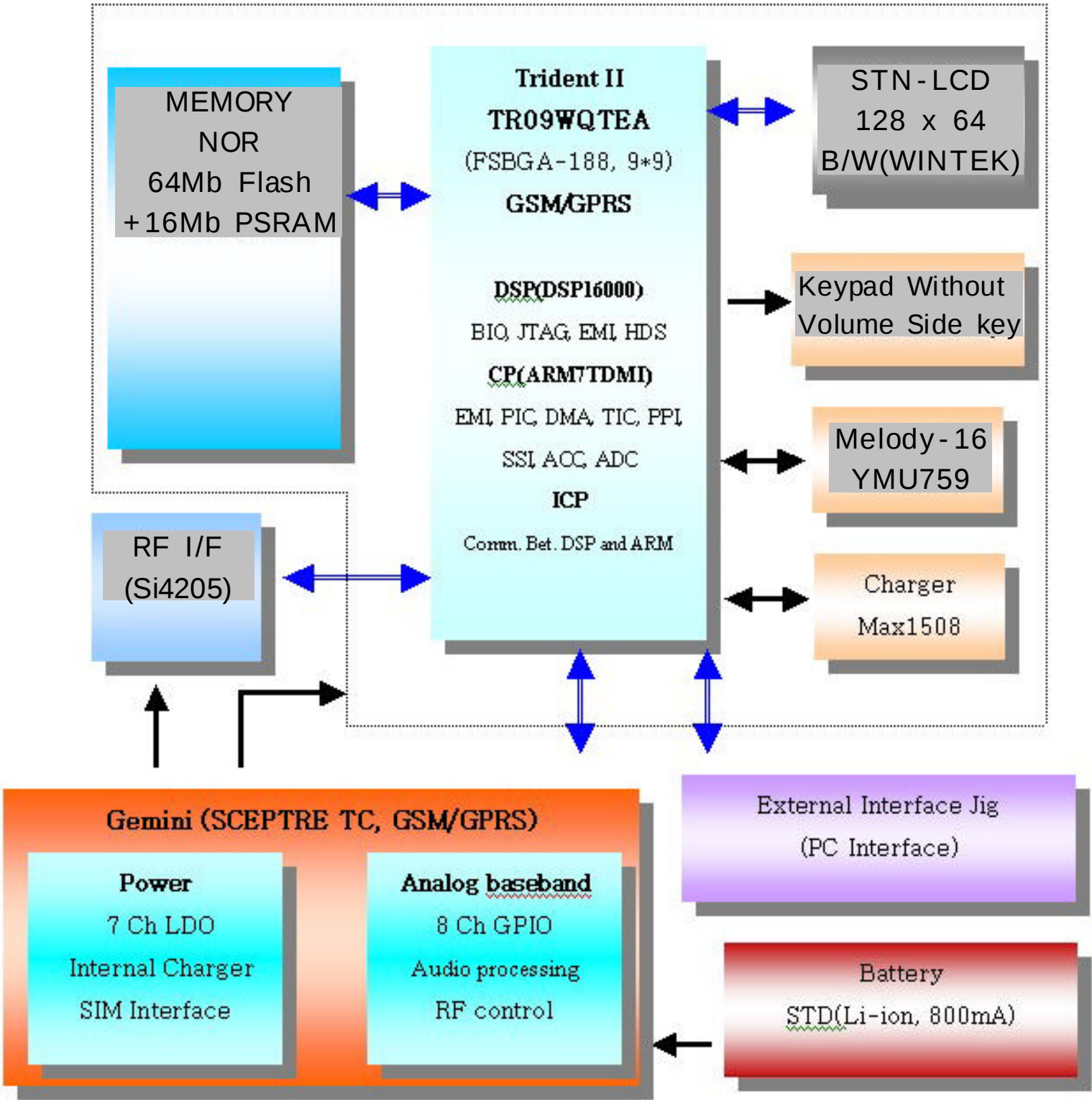
SEC CODE	Design LOC
2203-006093	C315
2203-006257	C121
2203-006257	C122
2203-006324	C104
2203-006324	C105
2404-001086	C511
2404-001239	C602
2404-001268	C123
2404-001281	C417
2404-001281	C433
2404-001305	C529
2404-001339	C509
2404-001348	C406
2703-002102	L401
2703-002201	L402
2703-002201	L405
2703-002624	L301
2703-002665	L403
2801-003747	OSC201
2809-001264	OSC401
2909-001236	U402
3705-001287	U401
3709-001335	CN101
3710-002017	CN601
4302-001130	BAT101
GH09-00028A	U201

5. SGH-N707 Block Diagrams

1. RF Solution Block Diagram

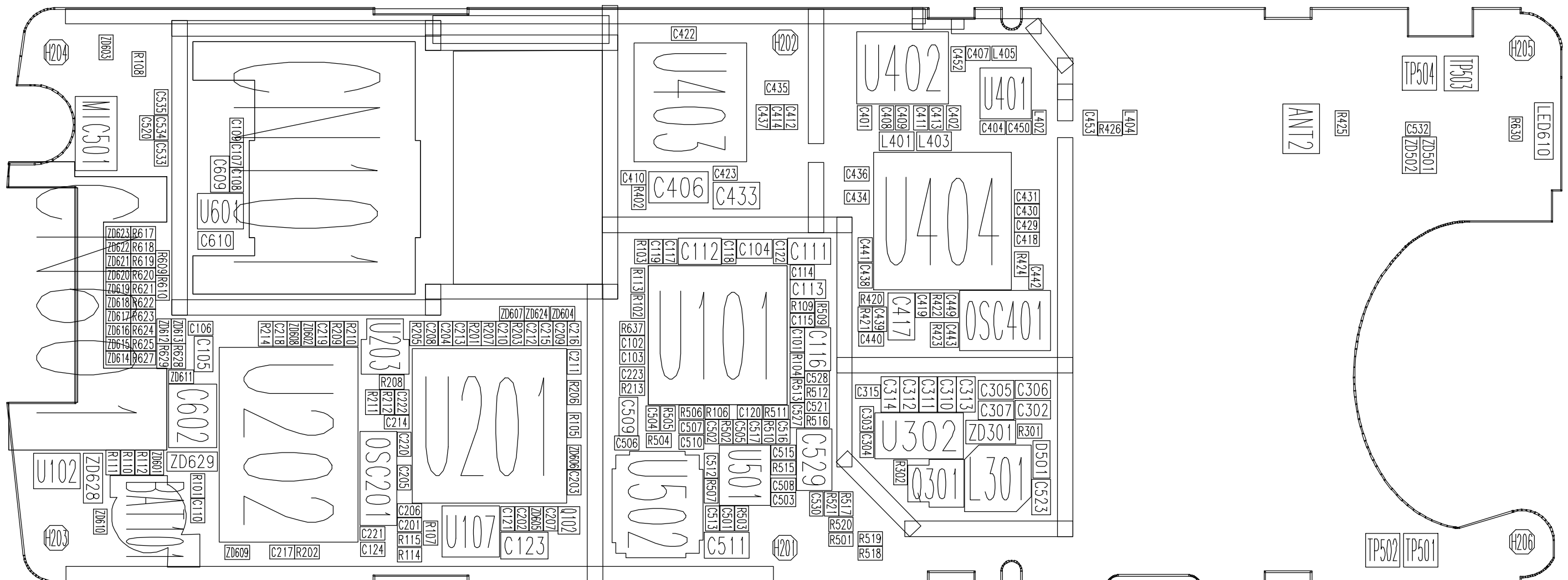


2. Base Band Solution Block Diagram

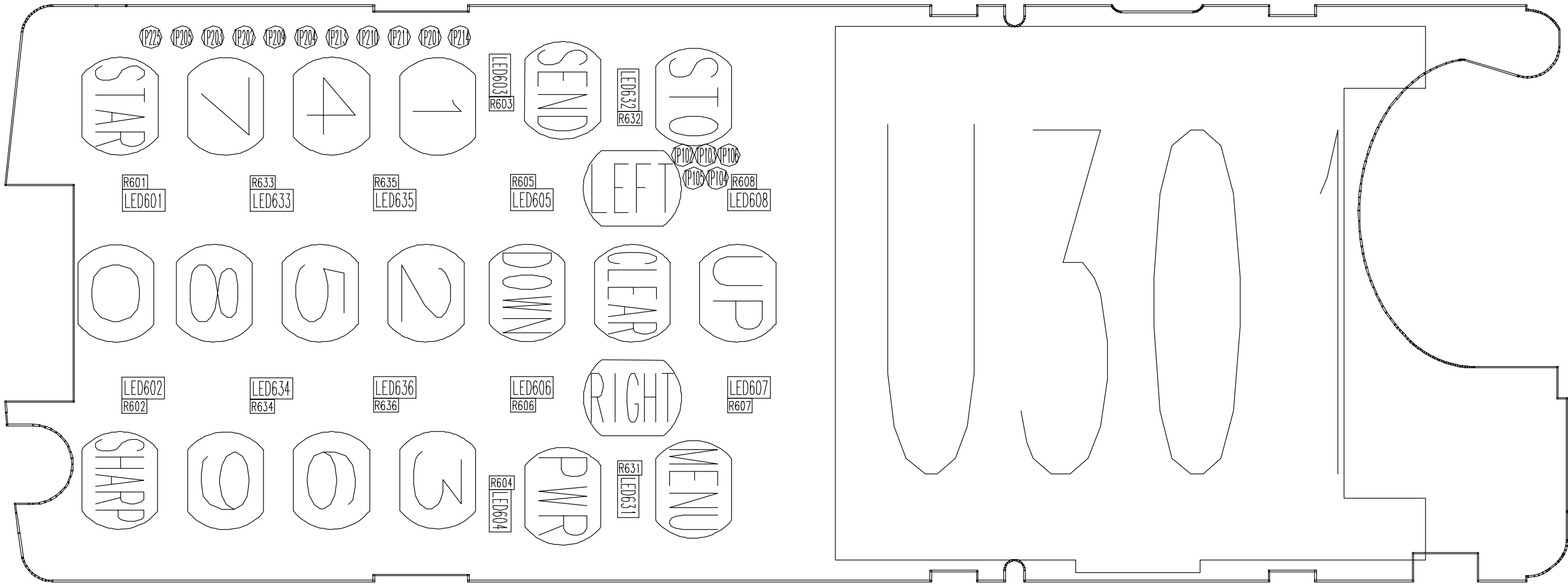


6. SGH-N707 PCB Diagrams

1. Main PCB Top Diagram

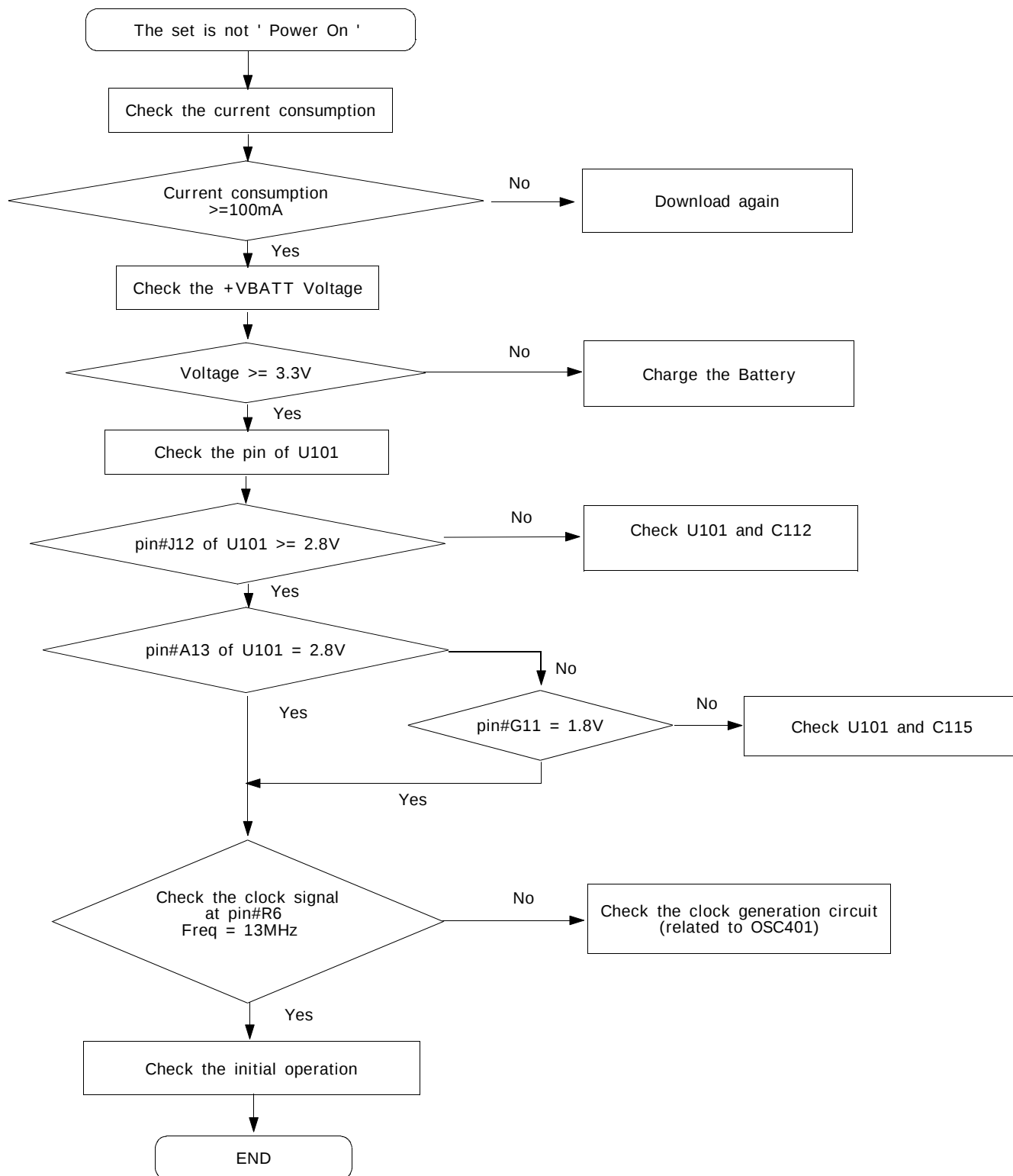


2. Main PCB Bottom Diagram

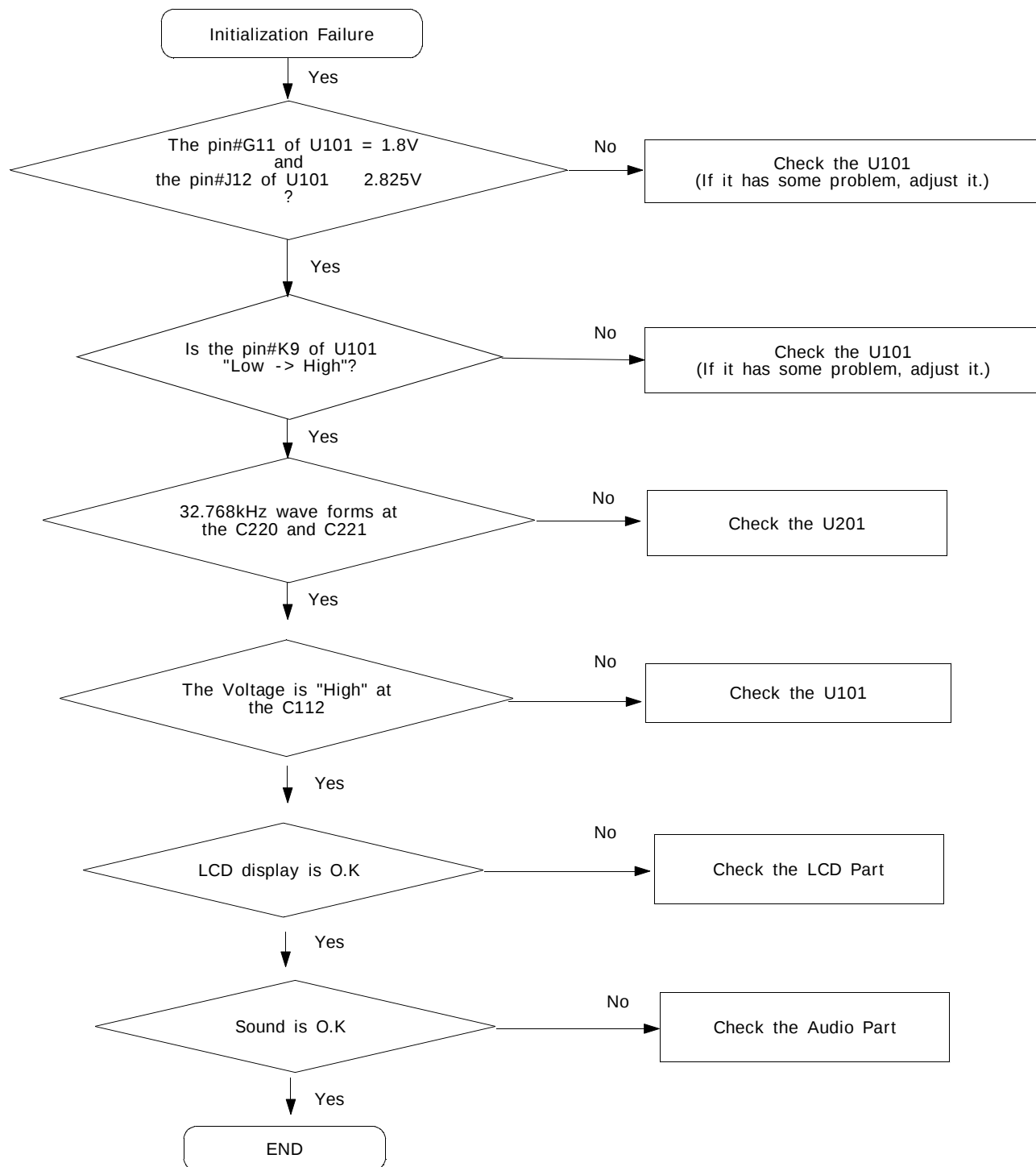


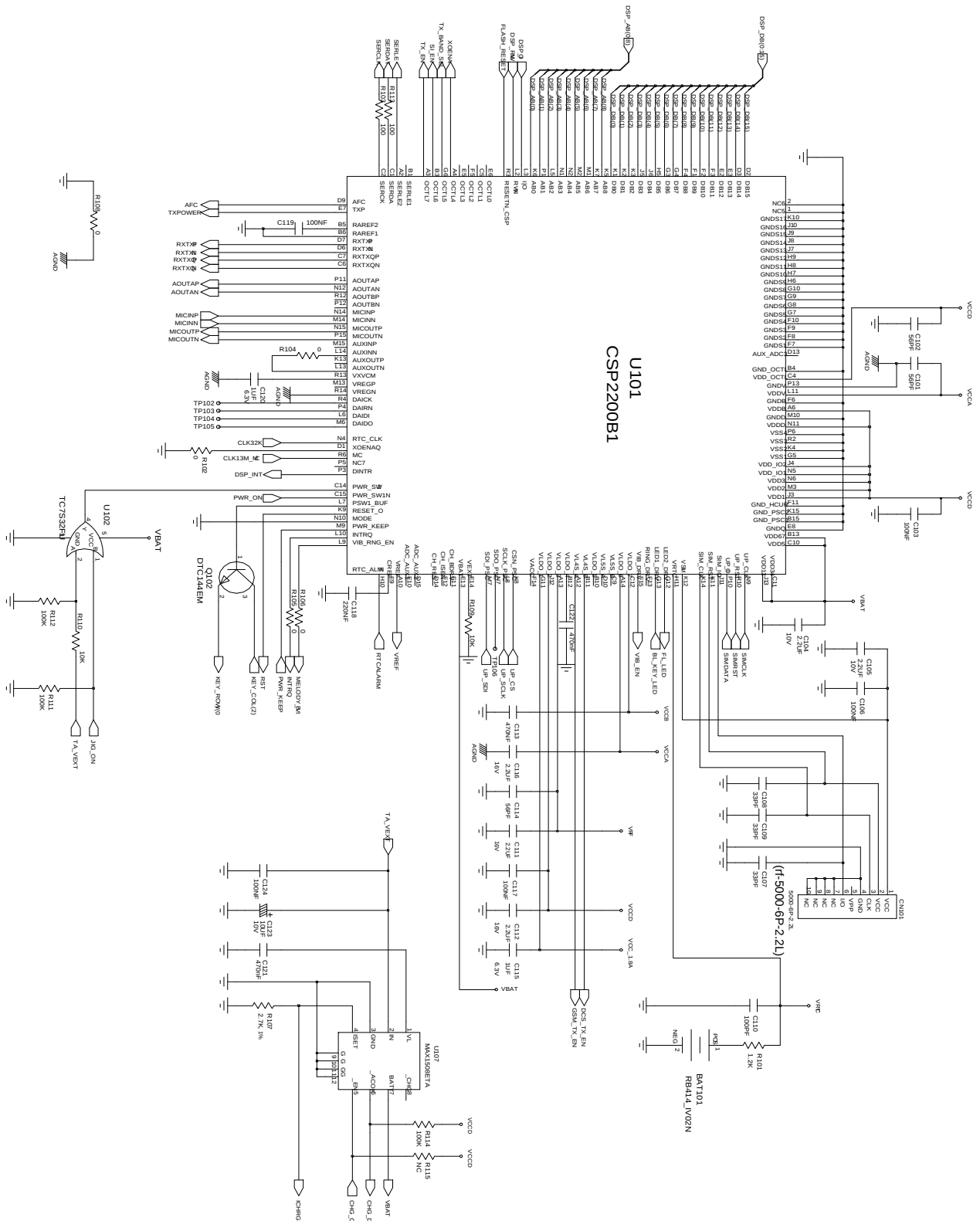
7. SGH-N707 Flow Chart of Troubleshooting

1. Power On

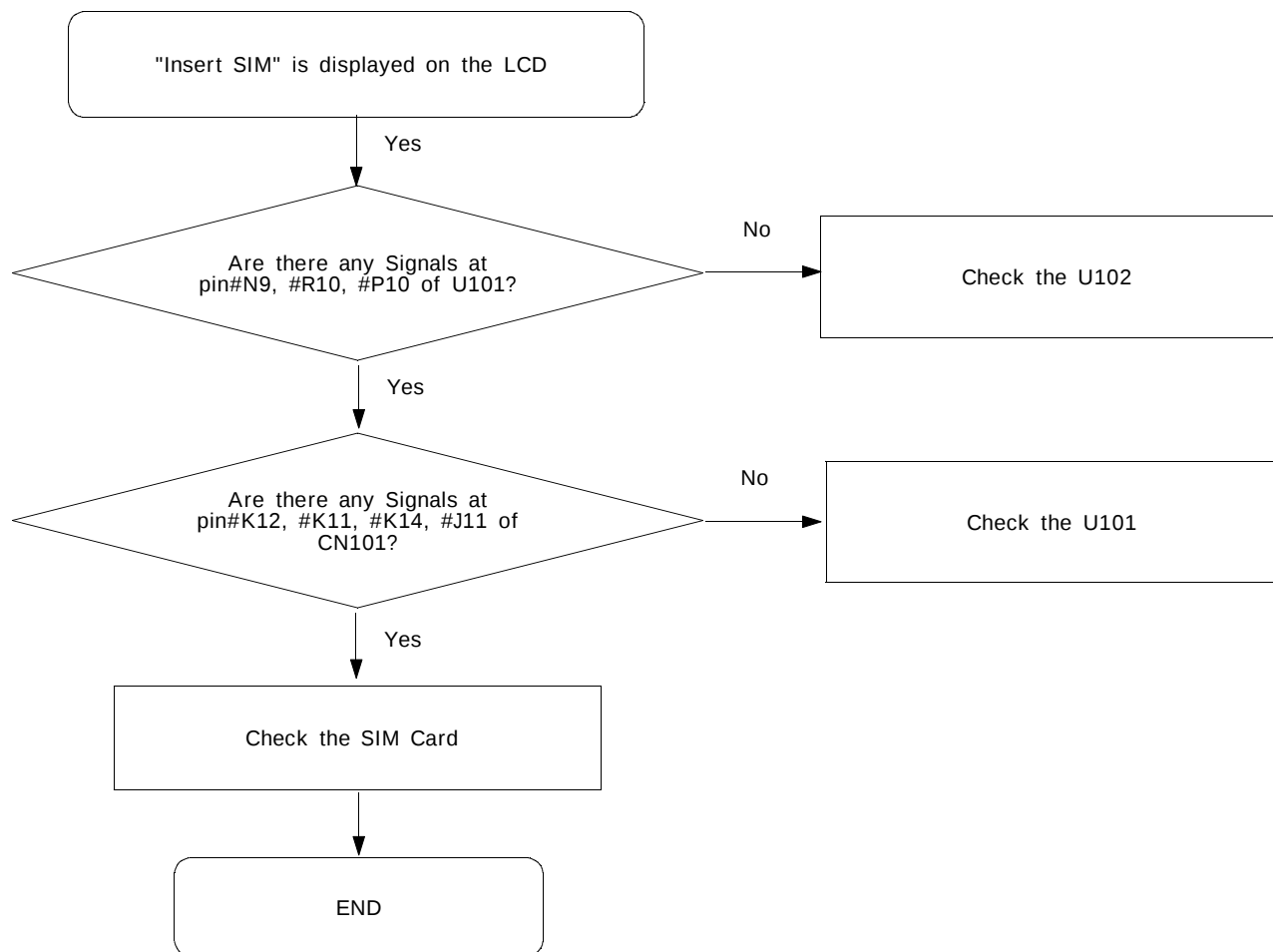


2. Initial

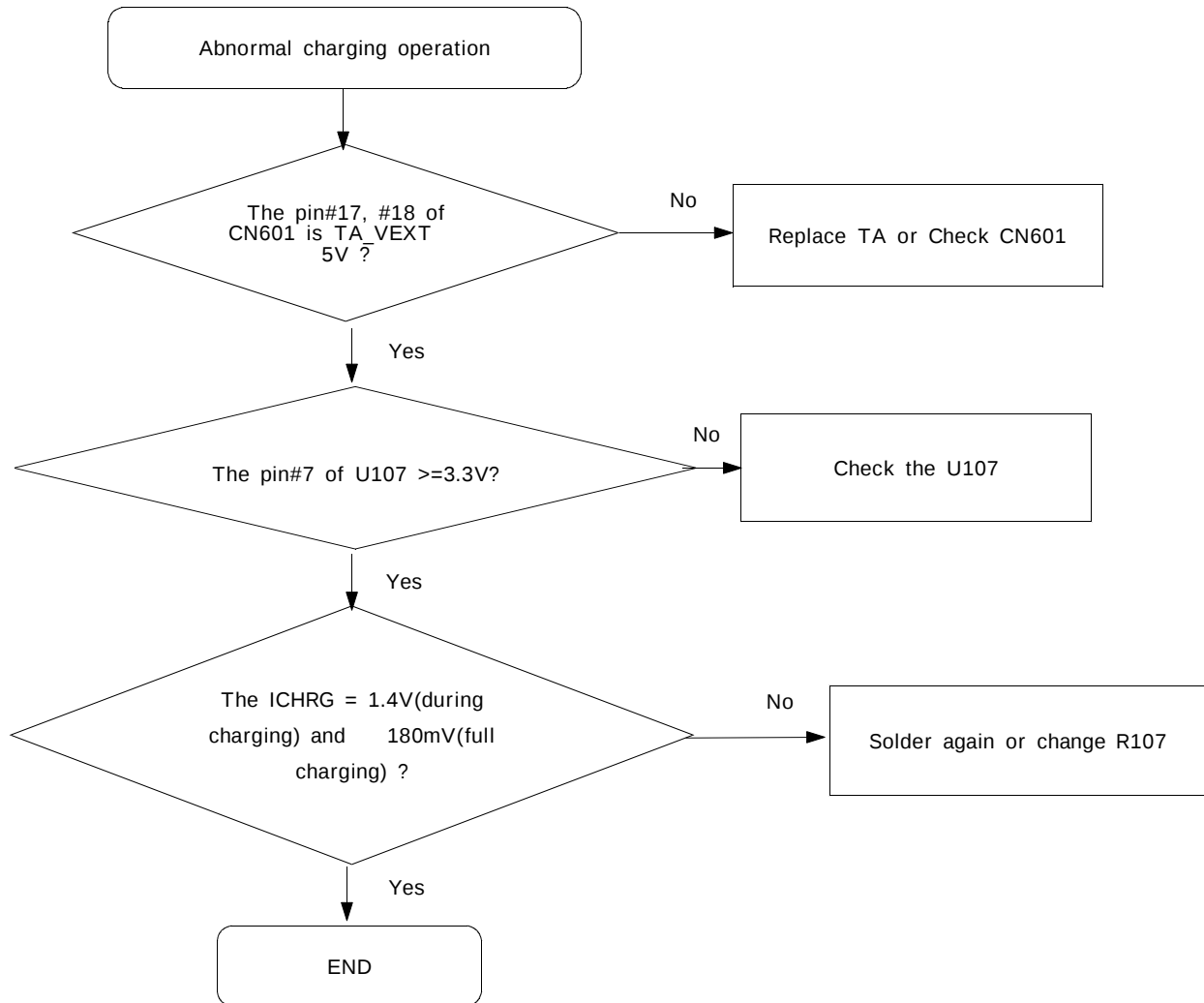




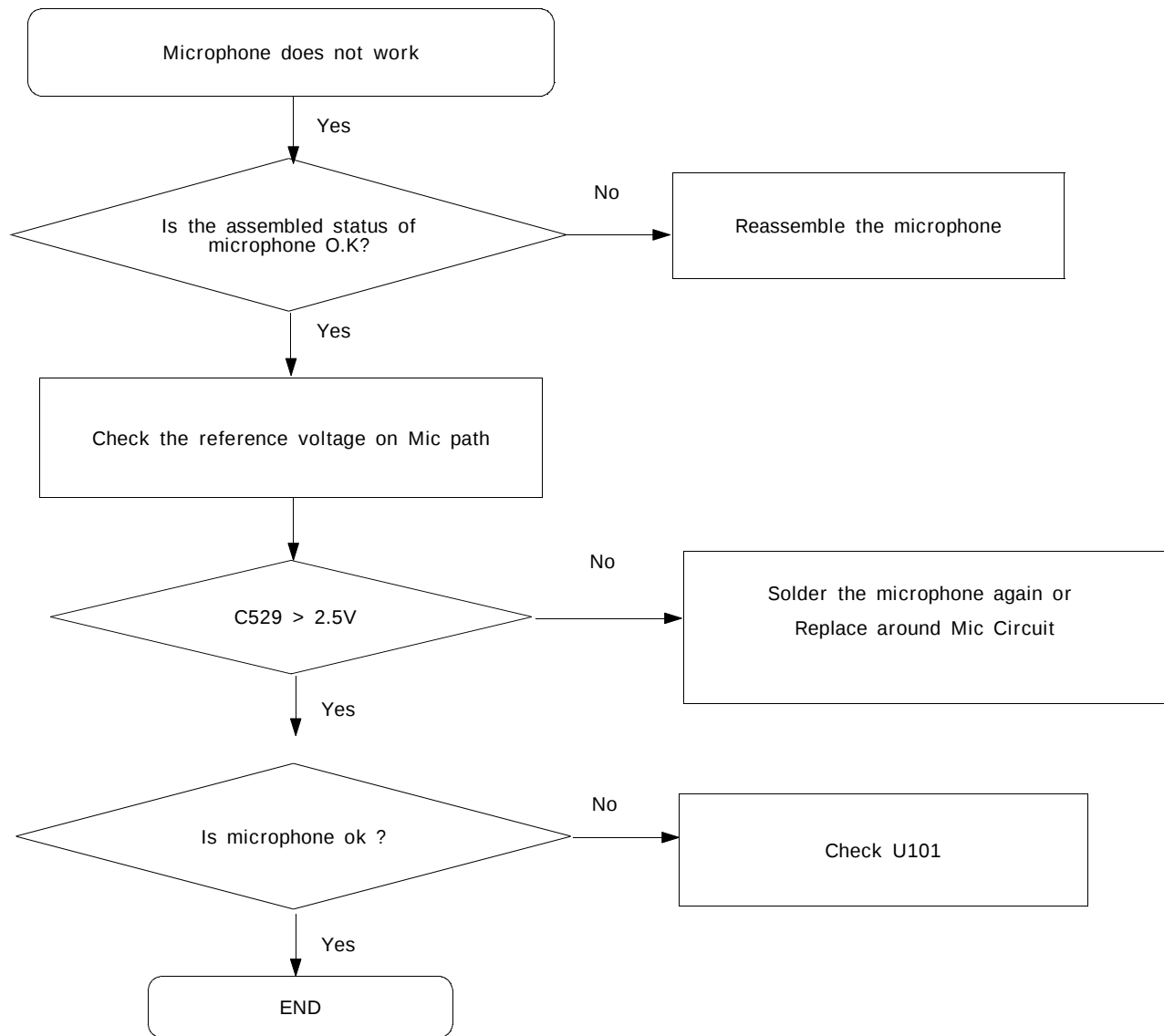
3. SIM Part



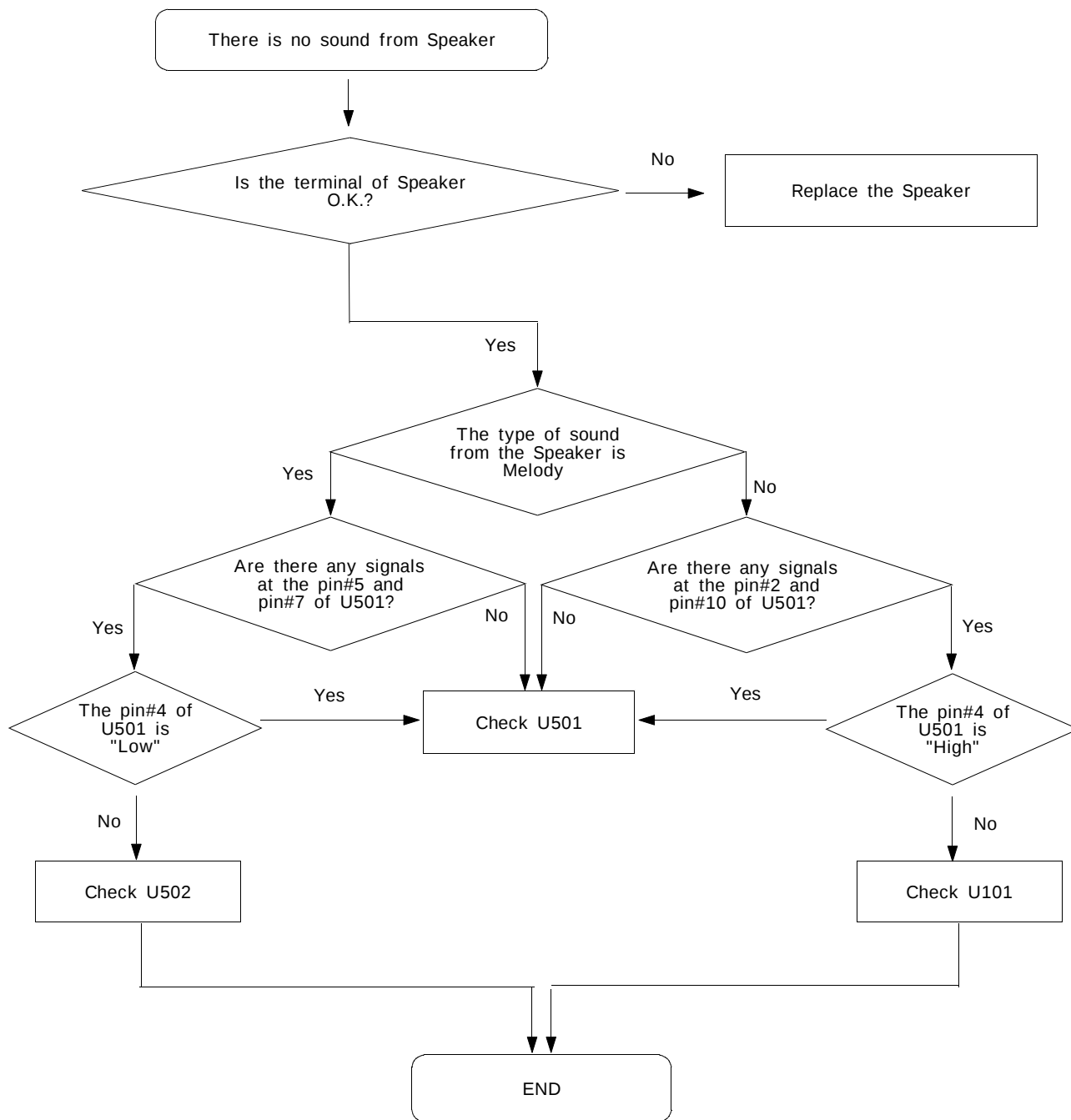
4. Charging Part

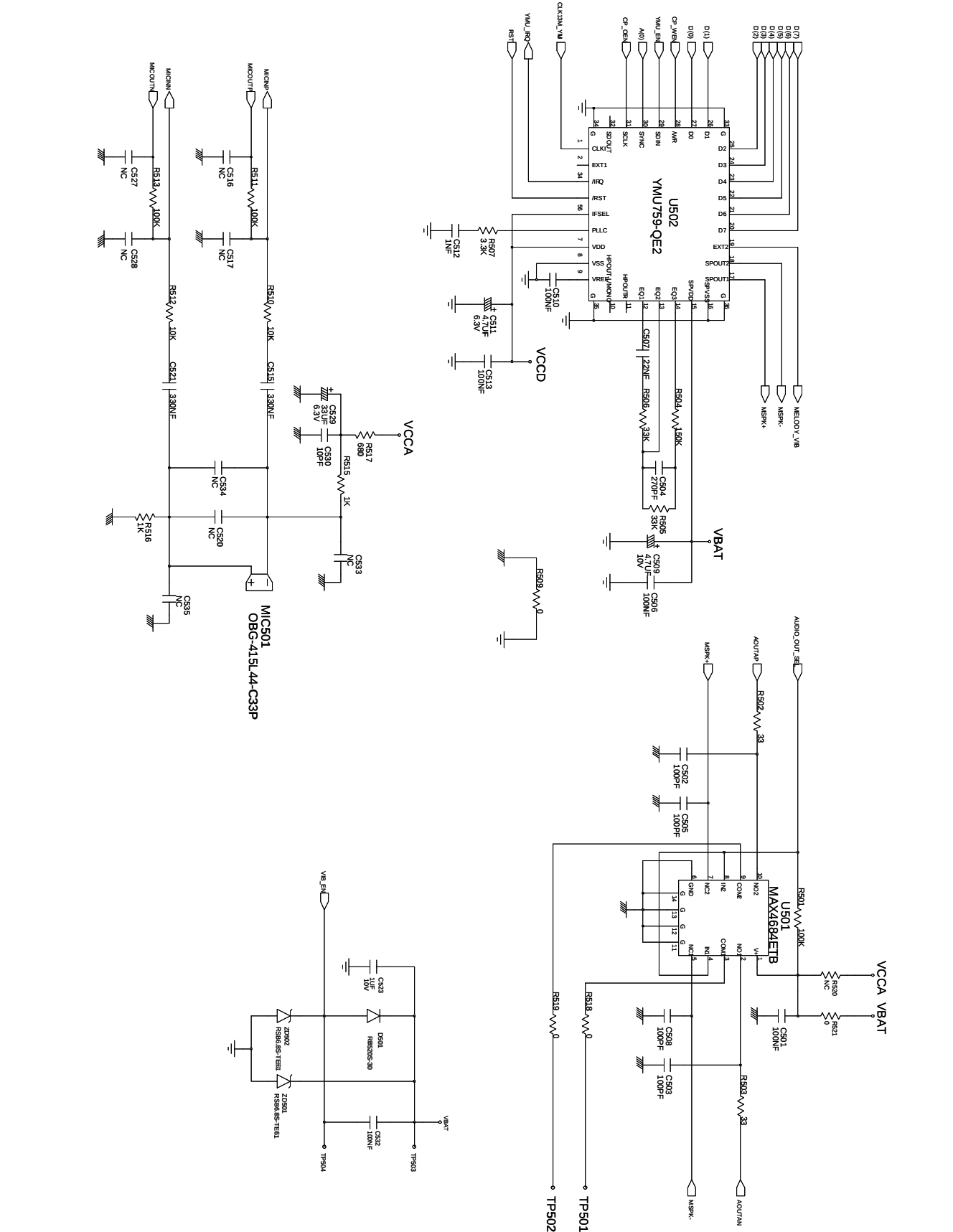


5. Microphone Part

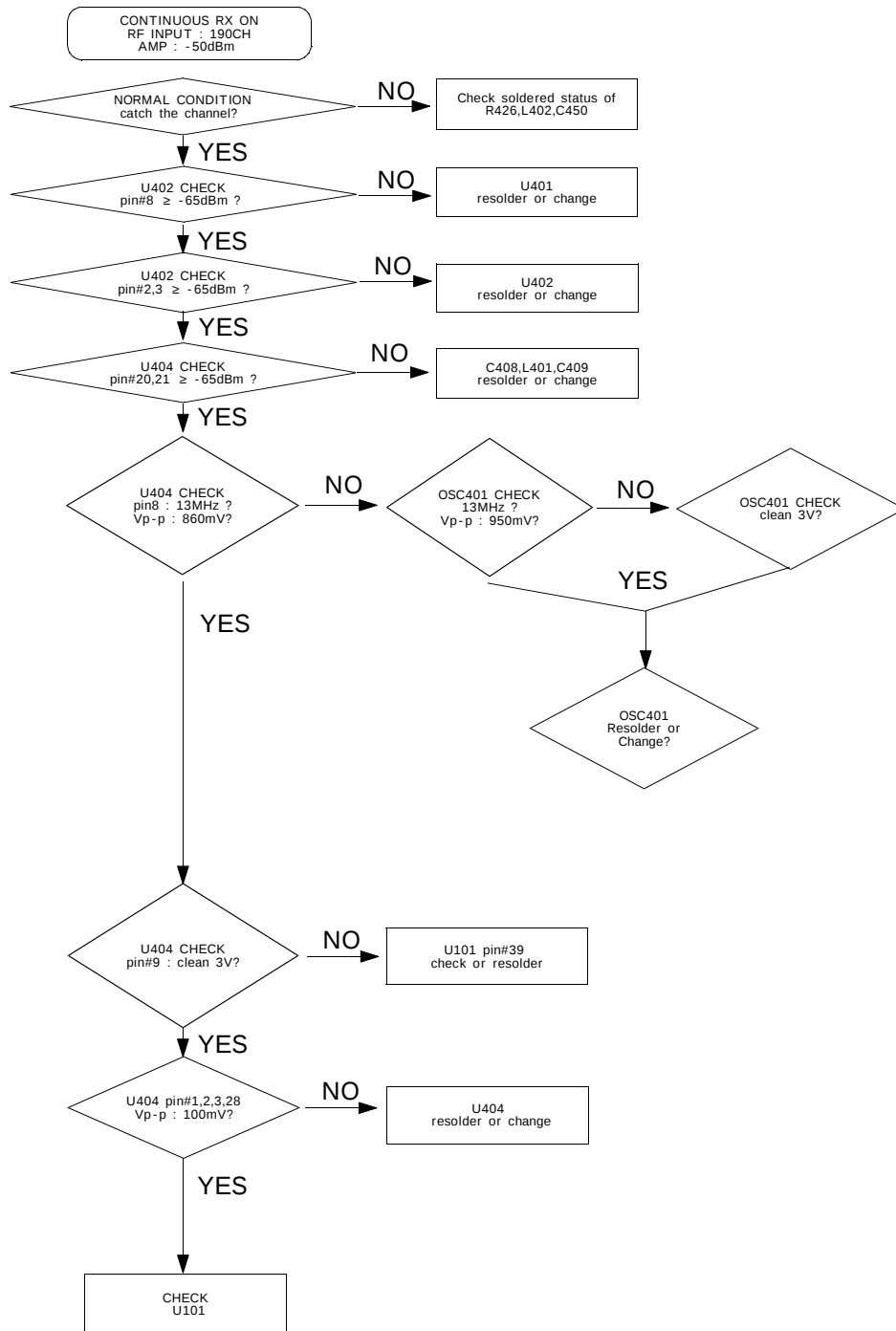


6. Speaker Part

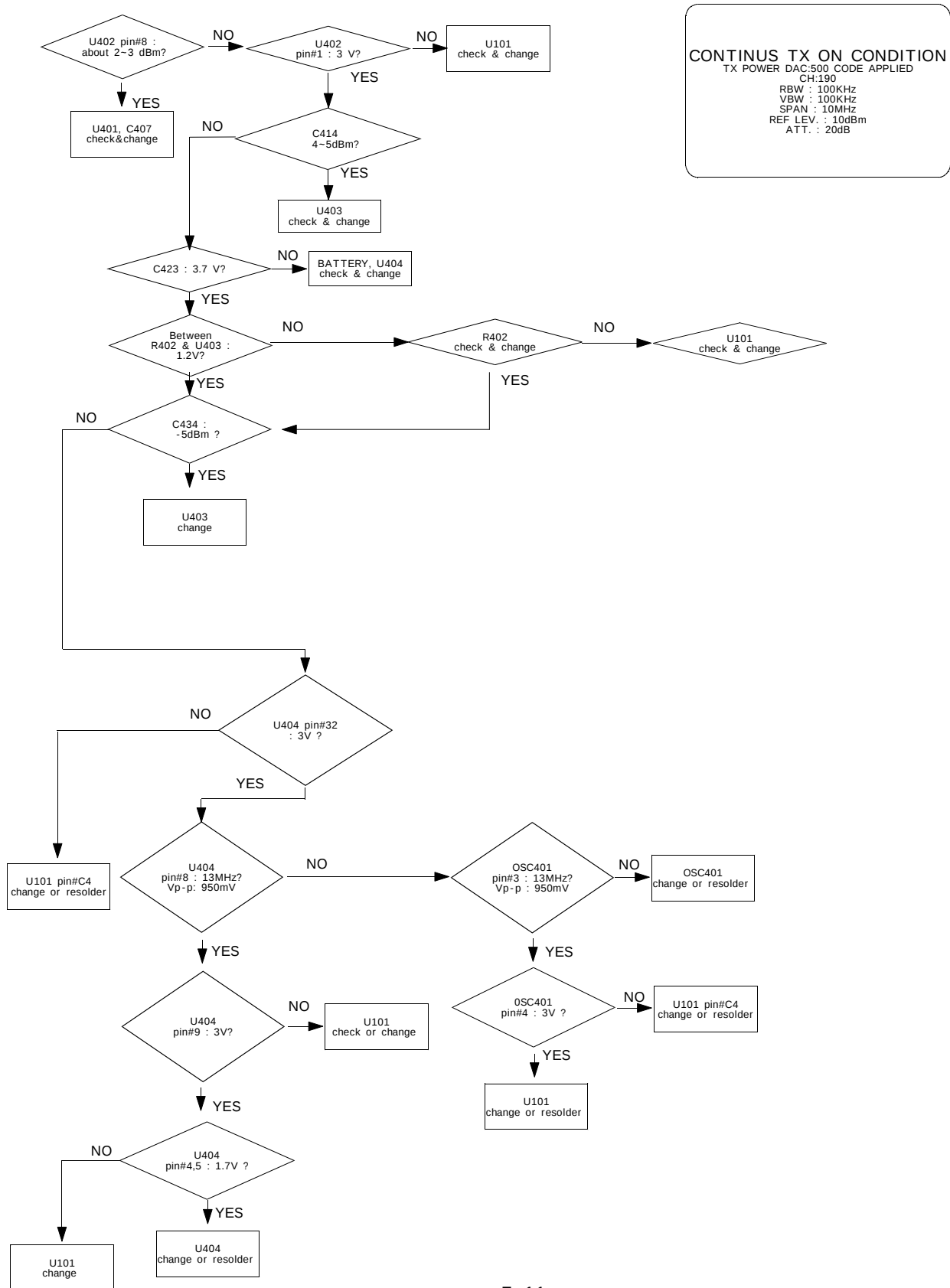




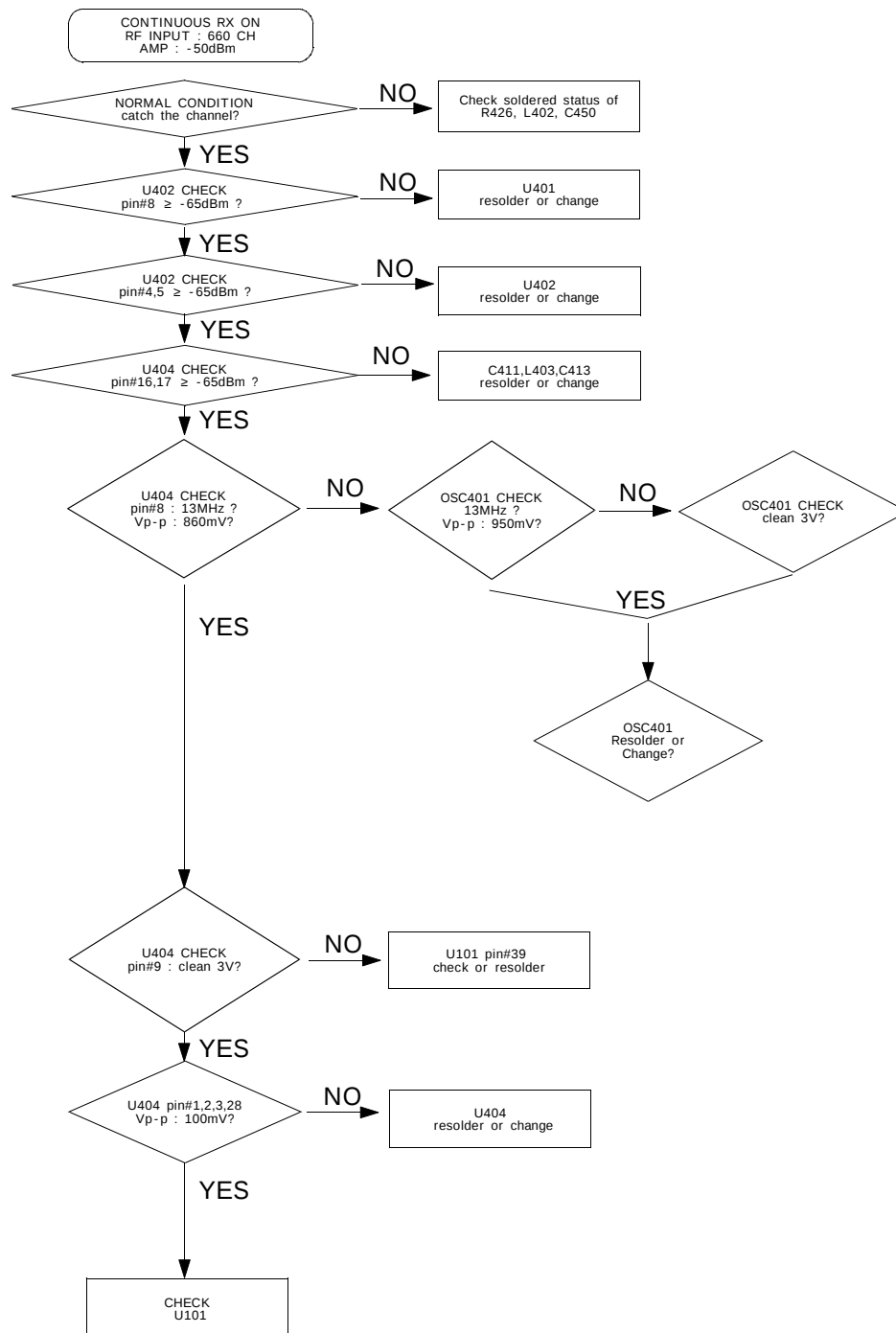
8. GSM Reciever



9. GSM transmitter



10. PCS Receiver



11. PCS transmitter

