Service Repair Documentation
Level 3 –S68

Release	Date	Department	Notes to change
R 1.0	23.02.2006	BenQ S CC CES	New document

Table of Content

1 Introduction

1.1 Purpose

This Service Repair Documentation is intended to carry out repairs on BenQ repair level 3.

1.2 Scope

This document is the reference document for all BenQ authorised Service Partners which are released to repair BenQ Mobile phones up to level 3.

1.3 Terms and Abbreviations

2 List of available level 3 parts

(according to Component Matrix V1.13 - check C-market for updates)

Product	RF Chipset	ID	Order Number	Description CM
S68	HIT	D1000	L50610-G6284-D670	IC SGOLD2 PMB8876 V2.1
S68	HIT	D1300	L50645-J4683-Y22	IC ASIC D1094ED-MOZART+ TWIGO4+
S68	HIT	D1301	L50610-B6189-D670	IC LOGIC 2 INPUT NAND NC7SP00L6X
S68	HIT	D1302	L50610-B6186-D670	IC LOGIC 2 INPUT AND NC7SZ08L6X
S68	HIT	D4002	L50645-K280-Y303	IC FEM HITACHI GSM900 1800 1900 (Fem-Type5)
S68	HIT	D4003	L50620-L6170-D670	IC TRANCEIVER HD155165BP PB Free
S68	HIT	D5100	L50610-U6122-D670	IC BLUETOOTH BRF6150 PB-FREE
S68	HIT	L1301	L50651-F5103-M1	COIL 10U (Co-Type9)
S68	HIT	L1303	L36140-F2100-Y6	COIL 0603 (Co-Type4)
S68	HIT	L1318	L36140-F2100-Y6	COIL 0603 (Co-Type4)
S68	HIT	L1320	L36140-F2100-Y6	COIL 0603 (Co-Type4)
S68	HIT	N1330	L50620-C6258-D670	IC DC DC BOOST CONVERTER LM2733
S68	HIT	N4001		IC MODUL PA PF0814 (PA-Type3) PB Free
S68	HIT	R4055	L36120-F4223-H	RESISTOR TEMP 22K (Res-Type7)
S68	HIT	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
S68	HIT	V1302	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
S68	HIT	V1303	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
S68	HIT	V1305	L36830-C1107-D670	TRANSISTOR SI5933 (Tra-Type2)
S68	HIT	V2100	L50640-D5084-D670	DIODE RB548W (Di-Type8)
S68	HIT	V2302	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
S68	HIT	V2801	L36840-C4061-D670	TRANSISTOR BC847BS BC846S (Tra-Type10)
S68	HIT	V4050	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
S68	HIT	X1400	L50634-Z97-C467	CONNECTOR BATTERY 3-POL X85
S68	HIT	X1504	L50634-Z93-C364	IO-JACK NANO 12-POL
S68	HIT	X1605	L50634-Z97-C406	CONNECTOR SIM CARD READER R65 (B)
S68	HIT	X2201	L50697-F5008-F340	CONNECTOR BOARD TO BOARD 20-POL B
S68	HIT	X2705	L50634-Z97-C363	CONNECTOR BOARD TO BOARD 14-POL. X75
S68	HIT	X4081	L36334-Z97-C334	CONNECTOR COAX SOCKET SWITCHED
S68	HIT	Z1001	L50645-F102-Y40	QUARZ 32,768KHZ (Q-Type4)
S68	HIT	Z1501	L50620-U6067-D670	FILTER EMI (Fi-Type8) PB Free
S68	HIT	Z1601	L50620-U6029-D670	FILTER EMI (Fi-Type6) PB Free
S68	HIT	Z4050	L36145-F260-Y17	QUARZ 26MHZ (Q-Type4)
S68	HIT	Z5100	L50645-K280-Y330	FILTER BP BLUETOOTH

3 Required Equipment for Level 3

- GSM-Tester (CMU200 or 4400S incl. Options)
- PC-incl. Monitor, Keyboard and Mouse
- Bootadapter 2000/2002 (L36880-N9241-A200)
- Adapter cable for Bootadapter due to ***new*** Lumberg connector (F30032-P226-A2)
- Troubleshooting Frame S68 (F30032-P711-A1)
- Power Supply
- Spectrum Analyser
- Active RF-Probe incl. Power Supply
- Oscilloscope incl. Probe
- RF-Connector (N<>SMA(f))
- Power Supply Cables
- Dongle (F30032-P28-A1) if USB-Dongle is used a special driver for NT is required
- BGA Soldering equipment

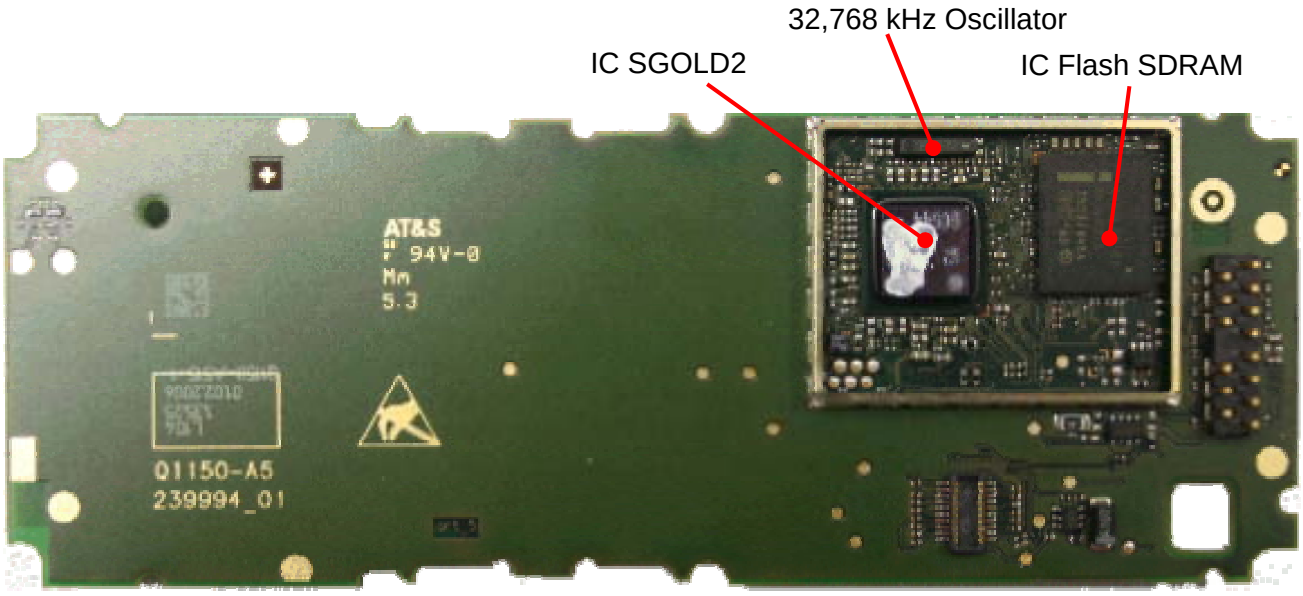
Reference: Equipment recommendation V2.0
(downloadable from the technical support page)

4 Required Software for Level 3

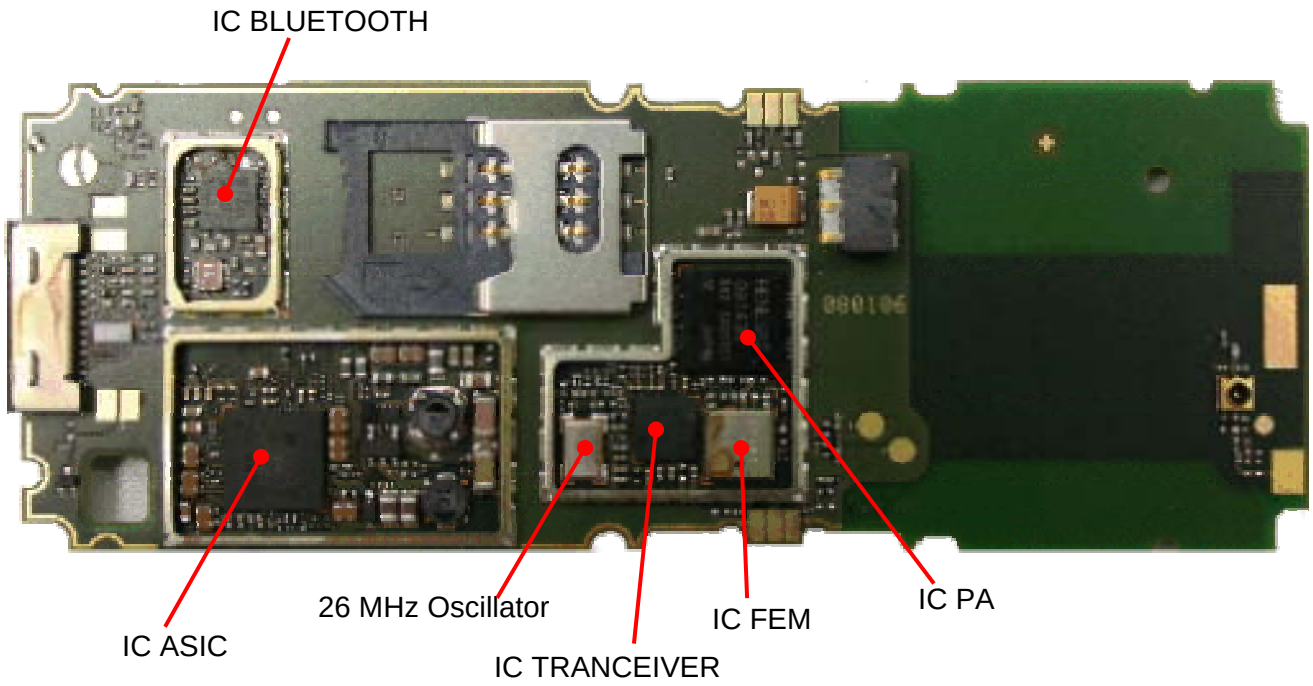
- Windows XP
- X-Focus version 2.04 or higher
- GRT Version 3.09 or higher
- Internet unblocking solution (JPICS)

5 PCB Main Board Overview

PCB Main Board Top Side



PCB Main Board Back Side



6 Radio Part

The radio part is realizes the conversion of the GMSK-HF-signals from the antenna to the baseband and vice versa.

In the receiving direction, the signals are split in the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which were generated in the logic part. After that the signals are amplified in the power amplifier.

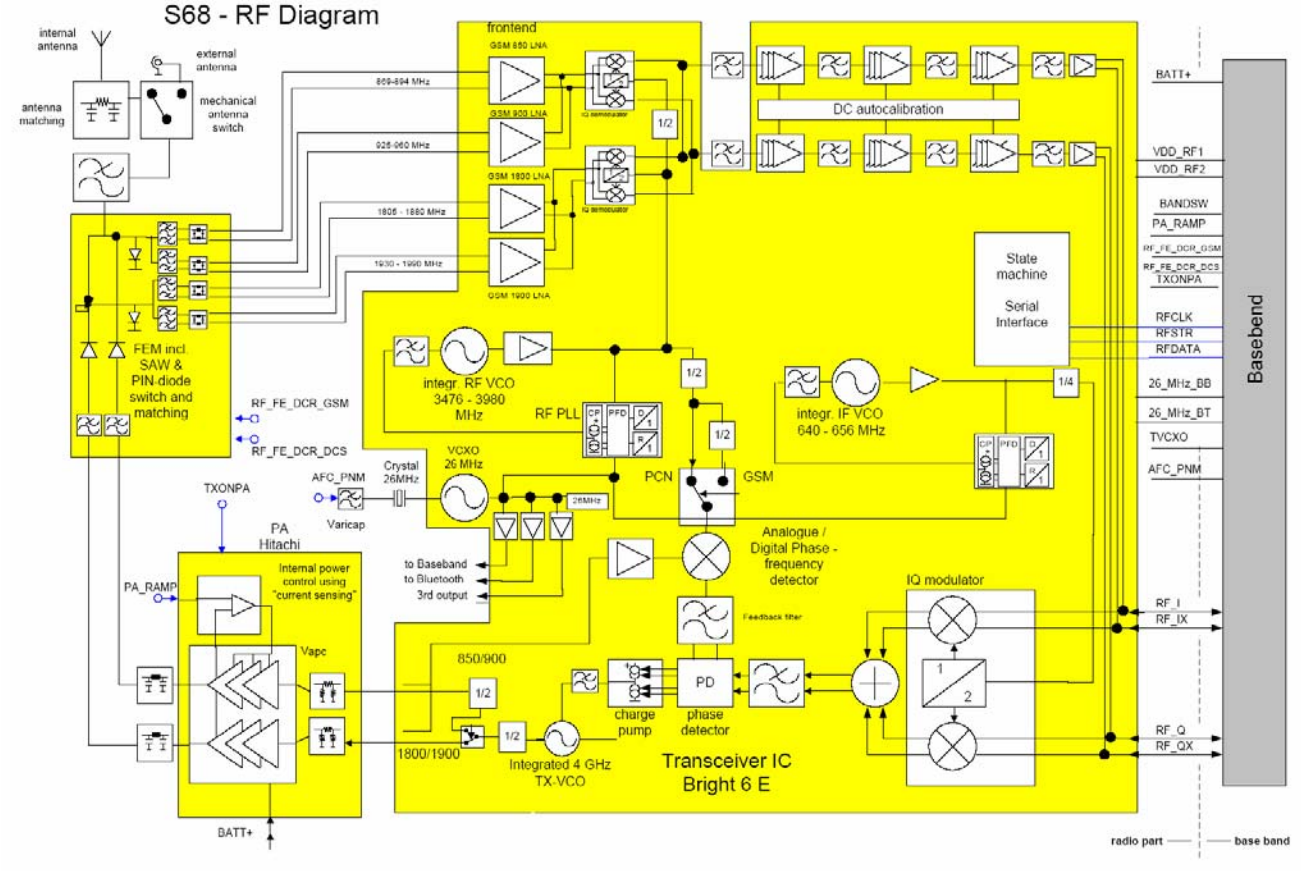
Transmitter and Receiver are never active at the same time. Simultaneous receiving in the EGSM900 and GSM1800 band is impossible. Simultaneous transmission in the EGSM900 and GSM1800 band is impossible, too. However the monitoring band (monitoring timeslot) in the TDMA-frame can be chosen independently of the receiving respectively the transmitting band (RX- and TX timeslot of the band).

The RF-part is dimensioned for triple band operation (EGSM900, DCS1800, PCS19000) supporting GPRS functionality up to multiclass 10.

The RF-circuit consists of the following components:

- Hitachi Bright 6E chip set (HD155165BP) with the following functionality:
  - PLL for local oscillator LO1 and LO2 and TxVCO
  - Integrated local oscillators LO1, LO2
  - Integrated TxVCO
  - Direct conversion receiver including LNA, DC-mixer, channel filtering and PGC-amplifier
  - 26 MHz reference oscillator
- Transmitter power amplifier with integrated power control circuitry
- Frontend-Module including RX-/TX-switch and EGSM900 / DCS1800 / PCS 1900 receiver SAW-filters
- Quartz and passive circuitry of the 26MHz VCXO reference oscillator

6.1 Block diagram RF part

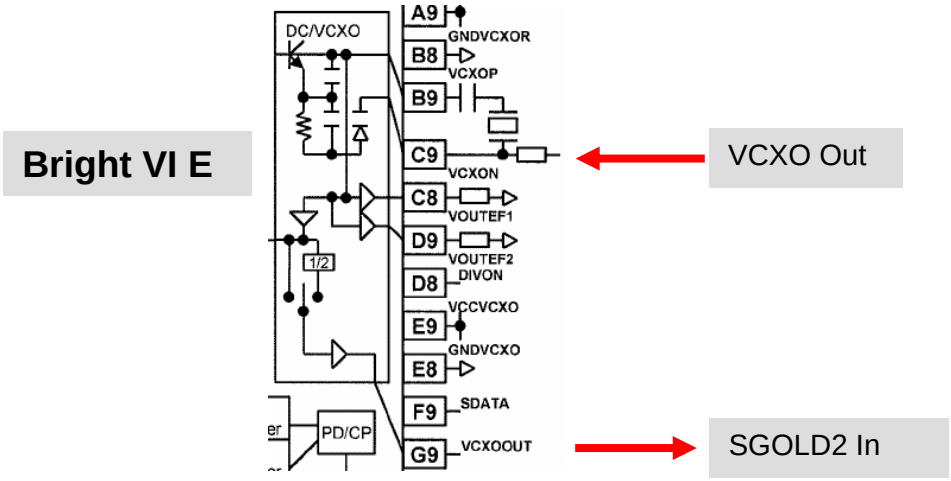


6.2 Power Supply RF-Part

The voltage regulator for the RF-part is located inside the ASIC D1300. It generates the required 2,8V “RF-Voltages” named VDD_RF1 and VDD_RF2. The voltage regulator is activated as well as deactivated via VCXOEN_UC (Functional K19) provided by the SGOLD2. The temporary deactivation is used to extend the stand by time.

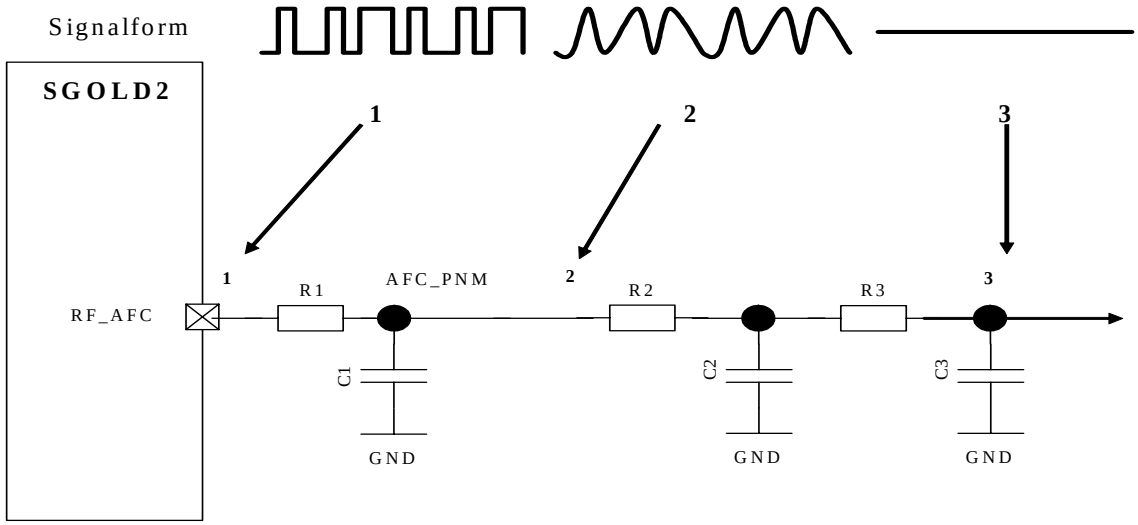
6.3 Frequency generation

The S68 mobile is using a Colpitts oscillator to generate the reference clock signal of 26MHz. As the S68 has to fulfil GPRS class 10 the active part is realised wit an external varactor diode. For temperature measurements of the VCXO a temperature-dependent resistance is used. The frequency of the reference oscillator can be adjusted by the SGOLD2 via a filtered PNM-modulated AFC-signal (RF_AFC). An active buffer stage is included in Bright VI E to give sufficient isolation between the base band chip and the RF-circuit.



The required voltage VDD_RF2 is provided by the ASCI D1300

Waveform of the AFC_PNM signal from SGOLD2 to Oscillator



Synthesizer: LO1

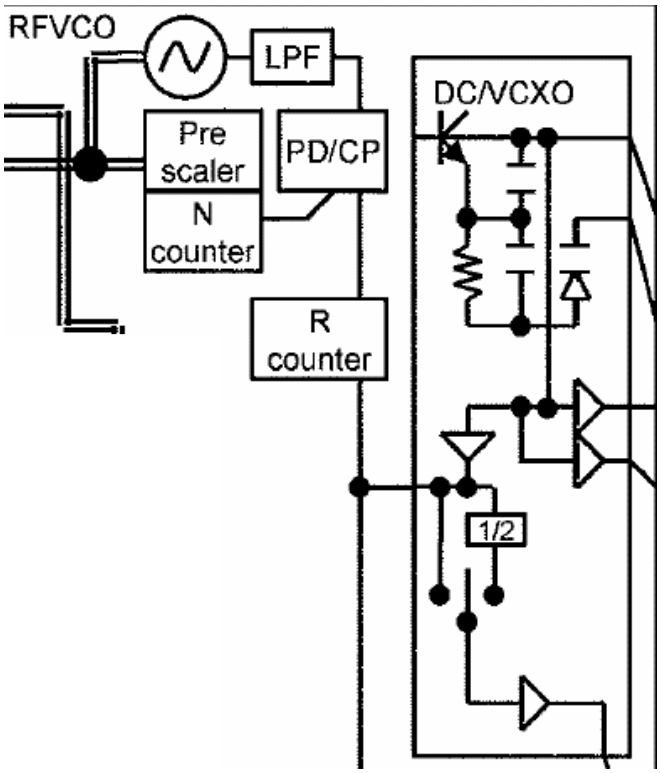
First local oscillator (LO1) consists of a PLL and VCO inside Bright (D4003) and an internal loop filter

RF PLL

The frequency-step is 400 kHz in GSM1800 mode and 800kHz in EGSM900 mode due to the internal divider by two for GSM1800 and divider by four for EGSM900. To achieve the required settling-time in GPRS operation, the PLL can operate in fastlock-mode a certain period after programming to ensure a fast settling. After this the loopfilter and currents are switched into normal-mode to get the necessary phasenoise-performance. The PLL is controlled via the tree-wire-bus of Bright VI E.

RFVCO (LO1)

The first local oscillator is needed to generate frequencies which enable the transceiver IC to demodulate the receiver signal and to perform the channel selection in the TX part. The VCO module is switched on with the signal PLLON. The full oscillation range is divided into 256 sub-bands To do so, a control voltage for the LO1 is used, gained by a comparator. This control voltage is a result of the comparison of the divided LO1 and the 26MHz reference Signal. The division ratio of the dividers is programmed by the SGOLD2, according to the network channel requirements.



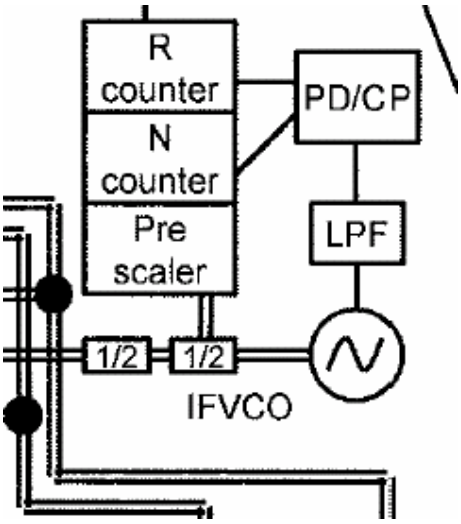
Matrix to calculate the TX and RX frequencies:

Band	RX / TX	Channels	RF frequencies	LO1 frequency	IF freq.
EGSM 900	Receive:	0..124	935,0 - 959,8 MHz	LO1 = 4*RF	
EGSM 900	Transmit:	0..124	890,0 - 914,8 MHz	LO1 = 4*(RF+IF)	80,0 MHz
EGSM 900	Receive:	975..1023	925,2 - 934,8 MHz	LO1 = 4*RF	
EGSM 900	Transmit:	975..1023	880,2 - 889,8 MHz	LO1 = 4*(RF+IF)	82,0 MHz
GSM 1800	Receive:	512..661	1805,2 - 1835,0 MHz	LO1 = 2*RF	
GSM 1800	Transmit:	512..661	1710,2 - 1740,0 MHz	LO1 = 2*(RF+IF)	80,0 MHz
GSM 1800	Receive:	661..885	1835,0 - 1879,8 MHz	LO1 = 2*RF	
GSM 1800	Transmit:	661..885	1740,0 - 1784,8 MHz	LO1 = 2*(RF+IF)	82,0 MHz
GSM 1900	Receive:	512..810	1930,2 - 1989,8 MHz	LO1 = 2*RF	
GSM 1900	Transmit:	512..810	1850,2 - 1909,8 MHz	LO1 = 2*(RF+IF)	80,0 MHz

Synthesizer: LO2

The second local oscillator (LO2) consists of a PLL and VCO inside Bright (D4003) and an internal loop filter. Due to the direct conversion receiver architecture, the LO2 is only used for transmit-operation. The LO2 covers a frequency range of at least 16 MHz (640MHz – 656MHz).
Before the LO2-signal gets to the modulator it is divided by 8. So the resulting TX-IF frequencies are 80/82 MHz (dependent on the channel and band). The LO2 PLL and power-up of the VCO is controlled via the tree-wire-bus of Bright (SGOLD2 signals RF_DAT; RF_CLK; RF_STR). To ensure the frequency stability, the 640MHz VCO signal is compared by the phase detector of the 2nd PLL with the 26Mhz reference signal. The resulting control signal passes the external loop filter and is used to control the 640/656MHz VCO.

The required voltage VDD_RF2 is provided by the ASIC D1300

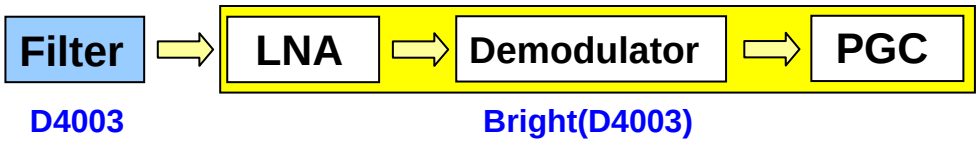


6.4 Receiver

Receiver: Filter to Demodulator

The band filters are located inside the frontend module (D4002). The filters are centred to the band frequencies. The symmetrical filter output is matched to the LNA input of the Bright .The Bright 6E incorporates three RF LNAs for GSM850/EGSM900, GSM1800 and GSM1900 operation. The LNA/mixer can be switched in High- and Low-mode to perform an amplification of ~ 20dB. For the “High Gain“ state the mixers are optimised to conversion gain and noise figure, in the “Low Gain“ state the mixers are optimised to large-signal behavior for operation at a high input level. The Bright performs a direct conversion mixers which are IQ-demodulators. For the demodulation of the received GSM signals the LO1 is required. The channel depending LO1 frequencies for 1800MHz/1900MHz bands are divided by 2 and by 4 for 850MHG/900MHz band. Furthermore the IC includes a programmable gain baseband amplifier PGA (90 dB range, 2dB steps) with automatic DC-offset calibration. LNA and PGA are controlled via SGOLD2 signals RF_DAT; RF_CLK; RF_STR (RF CTRL C16, C17, B18). The channel-filtering is realized inside the chip with a three stage baseband filter for both IQ chains. Only two capacitors which are part of the first passive RC-filters are external. The second and third filters are active filters and are fully integrated. The IQ receive signals are fed into the A/D converters in the EGAIM part of SGOLD2. The post-switched logic measures the level of the demodulated baseband signal and regulates the level to a defined value by varying the PGA amplification and switching the appropriate LNA gains.

From the antenna switch, up to the demodulator the received signal passes the following blocks to get the demodulated baseband signals for the SGOLD2:

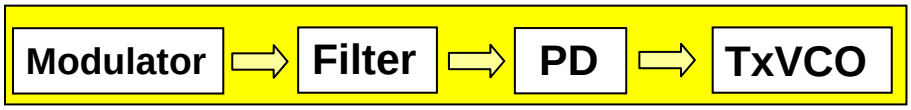


The required voltage VDD_RF2 is provided by the ASIC D1300

6.5 Transmitter

Transmitter: Modulator and Up-conversion Loop

The generation of the GMSK-modulated signal in Bright (D4003) is based on the principle of up conversion modulation phase locked loop. The incoming IQ-signals from the baseband are mixed with the divided LO2-signal. The modulator is followed by a lowpass filter (corner frequency ~80 MHz) which is necessary to attenuate RF harmonics generated by the modulator. A similar filter is used in the feedback-path of the down conversion mixer.
With help of an offset PLL the IF-signal becomes the modulated signal at the final transmit frequency. Therefore the GMSK modulated rf-signal at the output of the TX-VCOs is mixed with the divided LO1-signal to a IF-signal and sent to the phase detector. The I/Q modulated signal with a center frequency of the intermediate frequency is send to the phase detector as well.
The output signal of the phase detector controls the TxVCO and is processed by a loop filter whose components are external to the Bright. The TxVCO which is realized inside the Bright chip generates the GSMK modulated frequency.



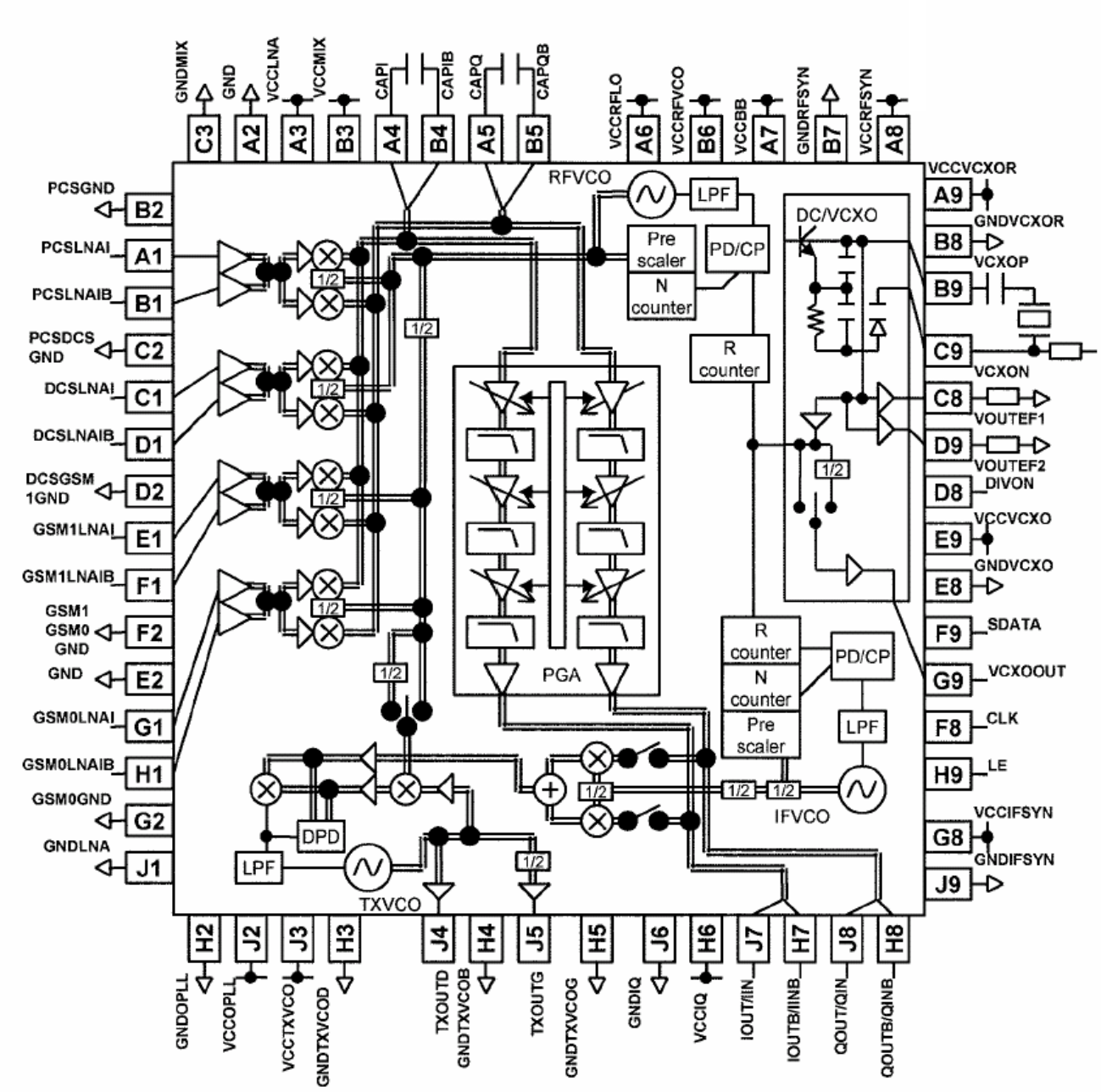
Bright(D4003)

The required voltage VDD_RF2 is provided by the ASIC D1300

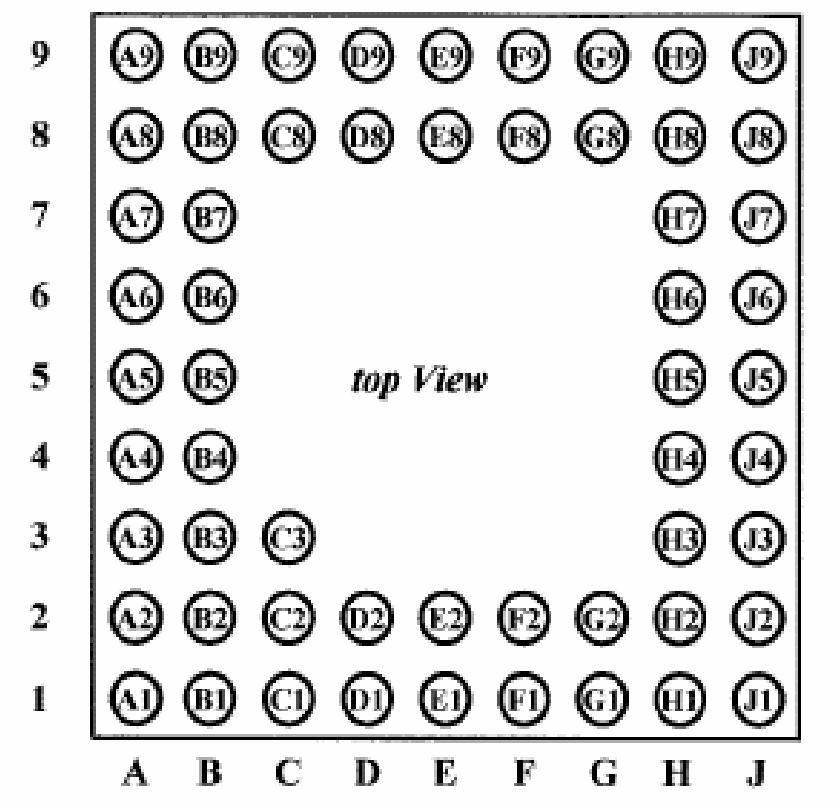
6.6 Bright IC Overview

BRIGHT 6E

IC Overview



IC top view (ball overview)



6.7 Antenna switch (electrical/mechanical)

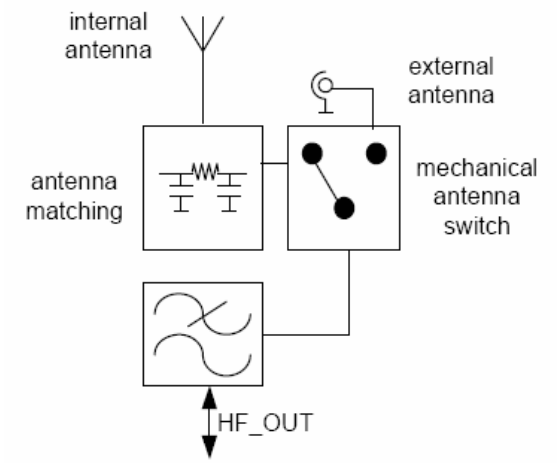
Internal/External <> Receiver/Transmitter
The S68 mobile have two antenna switches.

a) The mechanical antenna switch for the differentiation between the internal and external antenna which is used only for RF adjustments on the board.

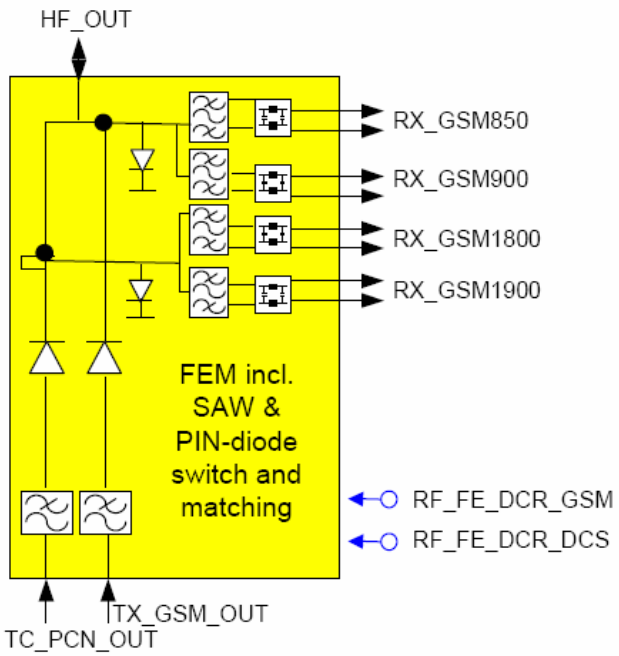
b) The electrical antenna switch, for the differentiation between the receiving and transmitting signals.

To activate the correct tx pathes of this diplexer, the SGOLD2 signals RF_FE_CTR_GSM and RF_FE_CTR_DCS are required.

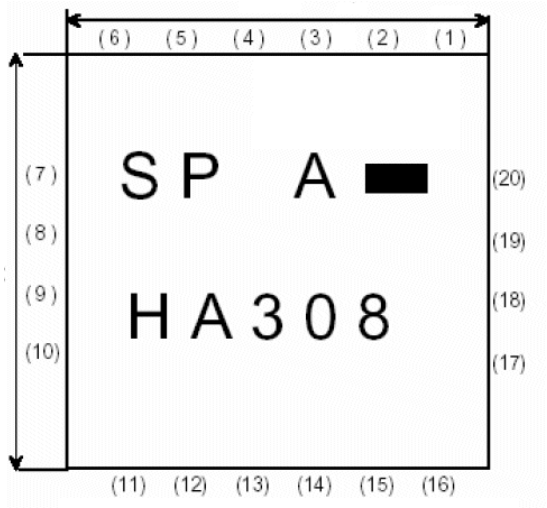
Internal/External antenna switch



The electrical antenna switch



Top View :



Switching Matrix:

select mode	Vsw 1	Vsw 2
GSM900/DCS1800/PCS1900 RX	Low	Low
EGSM TX	high	Low
DCS1800/PCS1900 TX	Low	High

Pin assignment:

1	**Antenna**	**15**	**EGSM900 RX1**
2	**GND**	**16**	**EGSM900 RX2**
3	**Vsw2 (DCS1800/PCS1900 TX control)**	**17**	**DCS1800 RX1**
4	**GND**	**18**	**DCS1800 RX2**
5	**DCS1800/PCS1900 TX**	**19**	**PCS1900 RX1**
6	**GND**	**20**	**PCS1900 RX2**
7	**GND**	**21**	**GND**
8	**GND**	**22**	**GND**
9	**GND**	**23**	**GND**
10	**GND**	**24**	**GND**
11	**GND**	**25**	**GND**
12	**GND**	**26**	**Vsw1 (EGSM900 TX control)**
13	**GND**	**27**	**EGSM900 TX**
14		**28**	**GND**

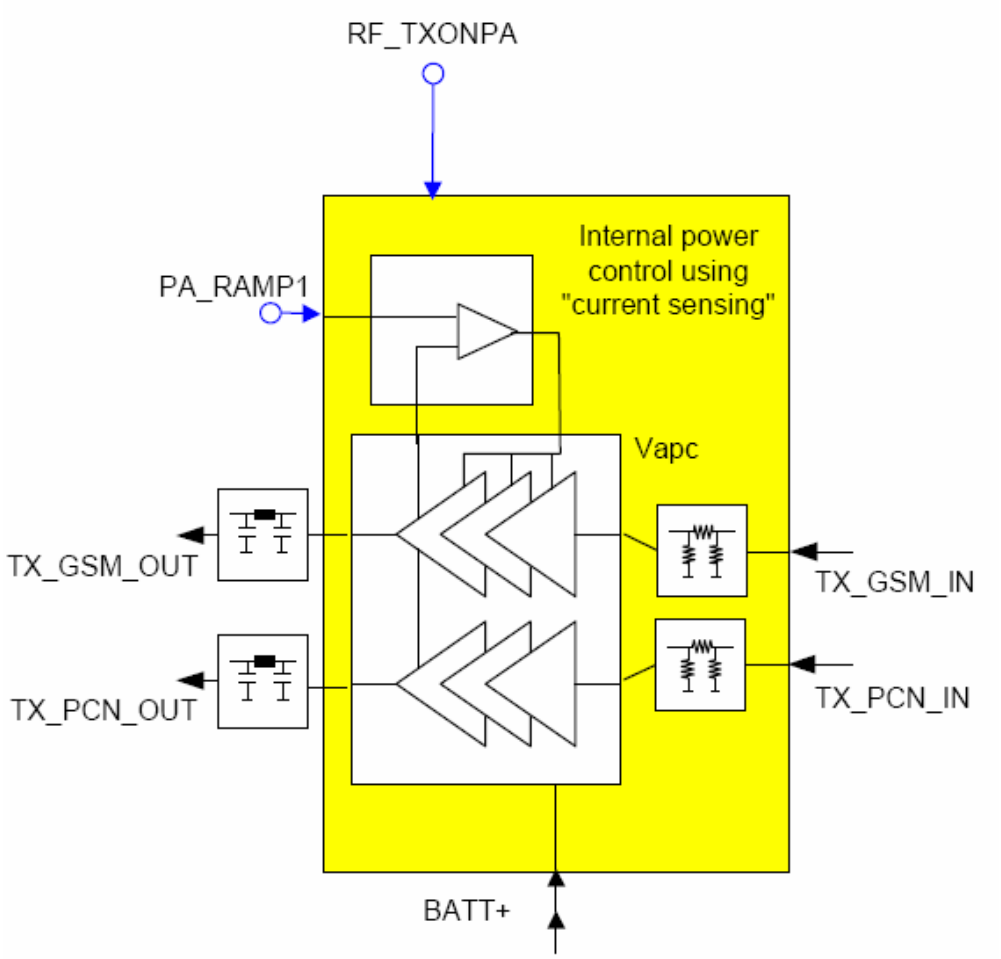
6.8 Transmitter: Power Amplifier

The output signals (PCN_PA_IN , and GSM_PA_IN) from the TxVCO are led to the power amplifier. The power amplifier is a PA-module N4001 from Hitachi. It contains two separate 3-stage amplifier chains GSM850/EGSM900 and GSM1800/GSM1900 operation. It is possible to control the output-power of both bands via one VAPC-port. The appropriate amplifier chain is activated by a logic signal RF_BAND_SW (TDMA Timer A18) which is provided by the SGOLD2.

To ensure that the output power and burst-timing fulfills the GSM-specification, an internal power control circuitry is use. The power detect circuit consists of a sensing transistor which operates at the same current as the third RF-transistor. The current is a measure of the output power of the PA. This signal is square-root converted and converted into a voltage by means of a simple resistor. It is then compared with the RF_RAMP1 (Analoq Interface L12) signal.

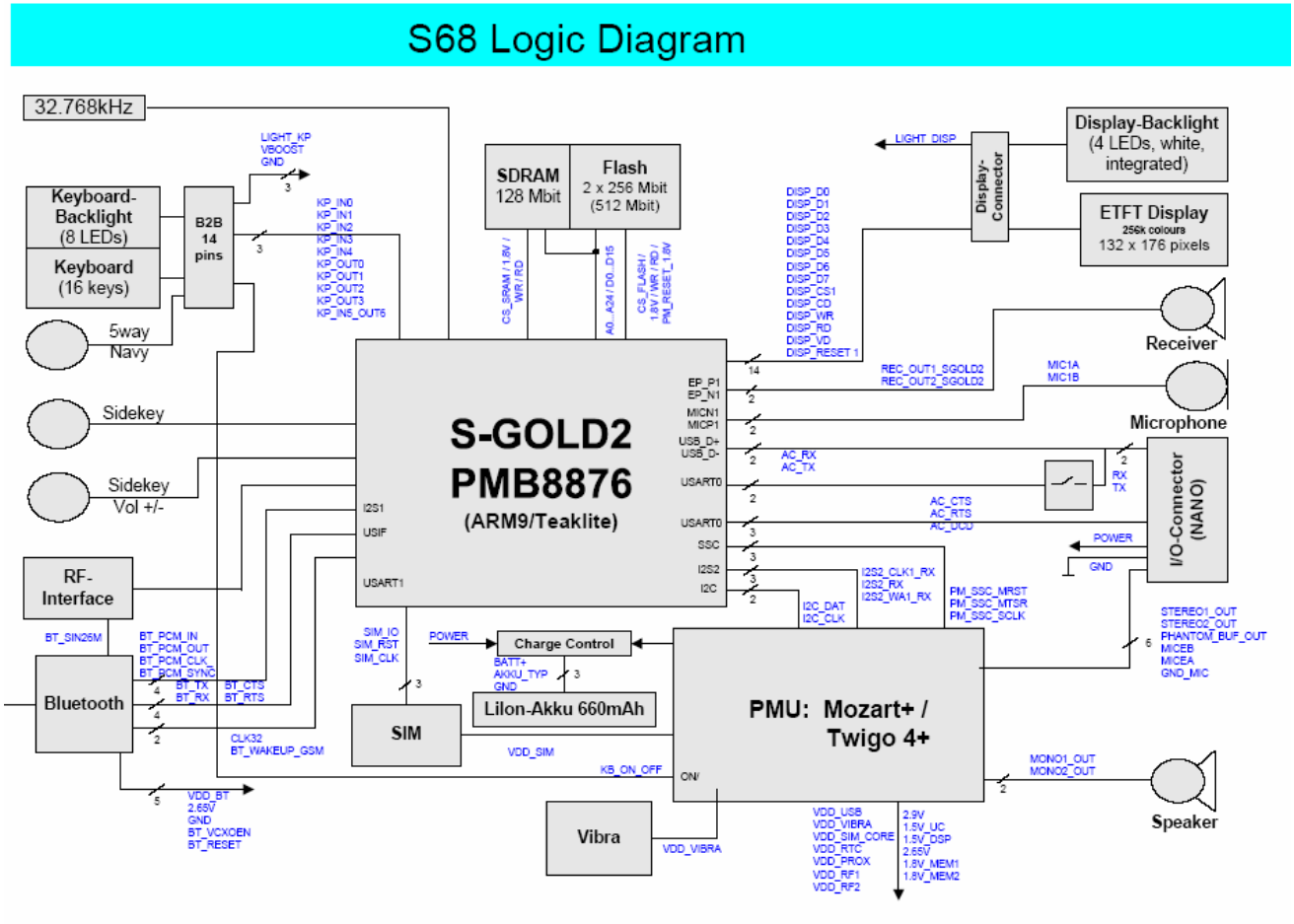
The N4001 is activated through the signal RF_TXONPA (TDMA Timer A18).

The required voltage BATT+ is provided by the battery.



7 Logic / Control

7.1 Overview Hardware Structure S68



7.2 SGOLD2

Baseband Processor SGOLD2 Features

Supported Standards

• EGPRS class 12 MCS 1..9
• GSM speech FR, HR, EFR and AMR-NB
• GSM data 2.4kbit/s, 4.8kbit/s, 9.6kbits, and 14.4kbit/s
• HSCSD class 10
• GPRS class 12 CS 1..4

Processing cores

• ARM926EJ-S 32 bit processor core with operating frequency up to 156 MHz for controller functions. The ARM926EJ-S includes an MMU, and the Jazelle Java extension for Java acceleration.
• TEAKLite® DSP core with operating frequency 138.67 MHz.

ARM-Memory

TEAKLite®-Memory (word: 16bit)

Shared Memory Blocks (word: 16bit)

Controller Bus System

TEAKLite® Bus System

Clock System

The clock system allows widely independent selection of frequencies for the essential parts of the S-GOLDliteTM. Thus power consumption and performance can be optimized for each application.

Functional Hardware blocks

• CPU and DSP Timers
• Programmable PLL with additional phase shifters for system clock generation
• GSM Timer Module that off-loads the CPU from radio channel timing
• GMSK Modulator according to GSM-standard 05.04 (5/2000)
– GMSK Modulator: gauss-filter with B*T=0.3
• Hardware accelerators for equalizer and channel decoding
• A5/1, A5/2, A5/3 Cipher Unit
(A5/3 added in S-GOLDliteTM V1.1)
• GEA1, GEA2, GEA3 Cipher Unit to support GPRS data transmission
(GEA3 added in S-GOLDliteTM V1.1)
• Advanced static and dynamic power management features including TDMA-Frame synchronous low-power mode and enhanced CPU modes (idle and sleep modes)
• Incremental Redundancy Memory for EDGE class 12 support
• GMSK / 8-PSK Modulator according to GSM-standard 05.04 (5/2000)
– GMSK Modulator: gauss-filter with B*T=0.3
– EDGE Modulator: 8PSK-modulation with linearised GMSK-pulse-filter
• MOVE coprocessor performing motion estimation for video encoding algorithms (H.263, MPEG-4)

Signal Processing Firmware Support

- FR, HR, EFR, and AMR
- data transmission channel codecs for 2.4, 4.8, 9.6 and 14.4 kbit/s
- HSCDS class 10 support
- GPRS class 12 support with coding schemes CS1..4
- Support for Handsfree, side- and signaling tone generation
- MMS-support
- EGPRS class 12 with modulation and coding schemes MCS1..9 (Release 5 compliant)
- Polyphonic ringer for up to 64 voices at sampling rates up to 48kHz
- 64 voices midi (pseudo) stereo
- enhanced audio visualization
- voice control

Interfaces and Features

- Keypad Interface for scanning keypads up to 8 rows and 8 columns
- Pulse Number Modulation output for Automatic Frequency Correction (AFC)
- Serial RF Control Interface; support of direct conversion RF
- 2 USARTs
- IrDA Controller
- 1 Serial Synchronous SPI compatible interfaces in the controller domain
- 1 Serial Synchronous SPI compatible interface in the TEAKLite® domain
- I2C-bus interface
- 2 bidirectional and one unidirectional I2S interface accessible from the TEAKLite®
- USB V1.1 mini host interface
- IEEE 1149.1 compliant JTAG port for Boundary Scan and debug
- ISO 7816 compatible SIM card interface
- Enhanced digital (phase linearity, adj/ co-channel interference) baseband filters, including analog prefilters and high resolution analog-to-digital converters.
- Digital and analog audio filters including wideband audio capable digital-to-analog and analog-to-digital converters.
- Audio front-end will be accessible from MCU (via shared memory) and the TEAKLite® (i.e. voice recognition and echo cancellation can run on TEAKLite®)
- Hifi Stereo voiceband with CD-Quality
- Separate analog-to-digital converter for various general purpose measurements like battery voltage, battery, VCXO and environmental temperature, battery technology,

t ransmission power, offset, onchip temperature, etc.

- Ringer support for highly oversampled PDM/PWM input signals for more versatility in ringer tone generation
- Differential VMIC generation
- RF power ramping functions
- DAI Interface according to GSM 11.10 is implemented via dedicated I2S mode
- 26 MHz master clock input
- External memory interface:
- Port logic for external port signals
- Comprehensive static and dynamic Power Management

– Various frequency options during operation mode
– 32 kHz clock in standby mode
– Sleep control in standby mode
– RAMs and ROMs in power save mode during standby mode

- Debug Features

- 2 General Purpose Timers with 3 32-bit timers
- Serial number
- A real time clock with alarm functions
- 2 capture/compare units with 16 channels
- A fast parallel Display Interface
- Camera Interface
- Programmable clock output for a camera
- An Multimedia/Secure Digital Card Interface (MMCI/SD; SDIO capable)
- A Flash Controller DMA Port (FCDP) supporting NAND flash
- A multimedia extension interface (MMIC-IF) supporting external hardware accelerator
- A Fast IrDA Interface
- A Universal Serial Interface (USIF) enabling asynchronous or synchronous serial data transmission.

7.3 SDRAM

The SDRAM (Synchronic Dynamic Random Access Memory) is for volatile data.

Memory Size:	128 Mbit (16 MByte)
Data Bus:	16Bit
IO / Core Voltage Supply:	typ. 1.8 V

7.4 FLASH

Code/Data Flash

It is a non-volatile-, re-programmable memory (SW-updateable), with a high performance interface. The mobile-SW can be executed directly. The Flash has an unchangeable serial number.

Memory Size:	512 Mbit (64 MByte)
Data Bus:	16 Bit
IO / Core Voltage Supply:	typ. 1.8V

7.5 SIM

SIM cards with supply voltages of 1.8V and 3V are supported..

7.6 Vibration Motor

The vibration motor is assembled in the lower case. The electrical connection to the PCB is realized with spring contacts.

8 Display

In S68 a display module with an intelligent graphic Liquid Crystal Display (LCD) is used.
The APUS display has a resolution of 132x176 pixels with a colour depth of 262144 colours (6-6-6 RGB). It contains an Active Matrix panel (Vertical Aligned Molecules) normally black panel. Driving technology is TFD, the controller is mounted on the glass (COG). Read functionality is enabled in order to perform status and/or ID read commands. Contrast adjust is fixed and cannot be changed by mobile user. The display enables wide viewing angle, no colour inversion, high contrast and high colour gamut. Luminance is using 4 high brightness white LED in series. FPC including components has been placed below the display module in order to reduce thickness of the module. Interconnection is done by 20-pin B2B connector.

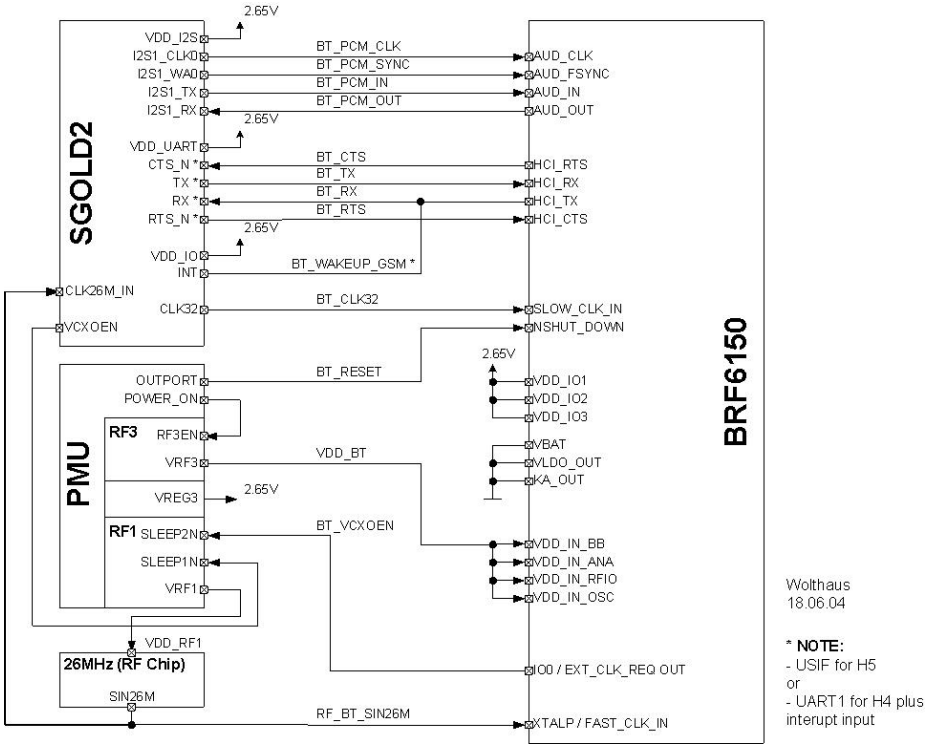
The display controller is supplied only with 2.9 V VDD. The 4 white LEDs are mounted in serial. The maximum current is set to 15 mA. The voltage for the 4 LEDs is about 18 V. No contrast adjustment is necessary. It is not possible to change the contrast by the mobile phone software. The colour adjustment of the display panel is also fixed by the supplier. The display contrast is pre-adjusted by the supplier and can be factory set in production/service.

9 Bluetooth

he Bluetooth Interface is based on the BRF6150 (D5100) from Texas Instruments. The BRF6150 is a single chip, this means the digital base-band and the radio part are implemented on the same silicon. The necessary firmware up to the HCI interface is stored in a diffusion ROM. The Bluetooth-Device-Address and the initialisation settings and values are stored in the GSM-Flash. During the start up of the BRF6150 the Mobile software writes this information to the device. Each Mobile Phone needs a unique Bluetooth-Device-Address.
The interface between the BRF6150 and GSM-Host-System consists of the following parts:

- Power supply (Mean power supply RF and base-band, I/O power supply)
- Clock supply (26MHz, 32,768 kHz)
- PCM interface (four lines, for voice sample)
- UART interface (four lines, for data and control)
- Miscellaneous (RESET, Wakeup optional for H4 protocol)

The following picture gives an overview about interfaces between the BRF6150 and the GSM Mobile system.



10 Power Supply

10.1 ASIC Mozart / Twigo4

The power supply ASIC will contain the following functions:

- Powerdown-Mode
- Sleep Mode
- Trickle Charge Mode
- Power on Reset
- Digital state machine to control switch on and supervise the uC with a watchdog
- 17 Voltage regulators
- 2 internal DC/DC converters (Step-up(not used) and Step-down converter)
- Low power voltage regulator
- Additional output ports
- Voltage supervision
- Temperature supervision with external and internal sensor
- Battery charge control
- TWI Interface (I^2C interface)
- Bandgap reference
- High performance audio quality
- Audio multiplexer for selection of audio input
- Audio amplifier stereo/mono
- 16 bit Sigma/Delta DAC with Clock recovery and I^2S Interface

10.1.1 Voltage Regulators and DC/ DC Converters

	Voltage	Current [mA]	start up default	Power supply name	Domain
REG 1	2,9V (+/-2%) 2,65V (+/-2%)	0...140	on	2.9V	SGOLD, Display
REG 2a	1,5V (+/-2%) 1,3V...1,5V in 100mV steps	0...300	on	1.5V_UC	not used
REG 2b	1,5V (+/-2%) 1,3V...1,5V in 100mV steps	0...100	on	1.5V_DSP	not used
REG 3	2,65V (+/-2%) 2,5V (+/-2%)	0...140	on	2.65V	SGOLD, IrDA, Bluetooth, Hall Switch, Audio/Video Interface
MEM REG1	1,8V (+/-2%) 2,5V (+/-2%)	0...250	on	1.8V_MEM1	SGOLD, Flash/SDRAM, Audio/Video Interface
MEM REG2	1,8V (+/-2%) 2,5V (+/-2%)	0...150	on	1.8V_MEM2	Flash/SDRAM
AUDIO REGa	2,9V (+/-2%)	0...190	off	VAUDREGA	internal use
AUDIO REGb	2,65 (+/- 2%)	0...30	off	n/a (Mozart internal use)	internal use
RF REG1	2,74V (+/-2%) 2,54V(+/-2%) 2,85V(+/-2%)	0...150	Sleep1_N or Sleep2_N	VDD_RF1	RF Tranceiver
RF REG2	1,53V(+/-2%) 2,7V (+/-2%) 2,85V(+/-2%)	0...180mA	depends on RF2_EN input	VDD_RF2	RF Tranceiver
RF REG3	1,8V(+/-2%) 2,7V (+/-2%) 2,85V(+/-2%)	0...180	depends on RF3_EN input	VDD_BT	Bluetooth
AFC REG	2,65V (+/-2%)	0...2	always active	VDD_AFC	SGOLD
LP_REG	2,0V	0...2	always active	VDD_RTC	SGOLD
SIM REGa	2,9V (+/-2%) 1,8V (+/-2%)	0...70	off	VDD_SIM	SIM
SIM REGb	2,9V (+/-2%) 1,8V (+/-2%)	0...10	on	n/a (not used)	not used
USB REG	3,1V (+/-2%)	0...40	on	VDD_USB	SGOLD
VIBRA	2,8V (+/-2%)	0...140	off	VDD_VIBRA	Vibra
DCDC STEP DOWN (BUCK-Converter)	1,5V 2,1V	700	on	VBUCK	SGOLD

10.1.2 Power Management Concept

A double MOSFET V1305 is placed between the battery and the charge pin at the IO connector. This enables both normal charging as well as reverse supply from the battery to external accessories, requiring power from the phone. The PA is supplied directly from the battery. A number of different LDOs supply different parts of the phone. The external LDO's are supplied directly from the battery.

A DC/DC step-down converter with additional input filters was foreseen to supply the LDOs with the highest current limitation (VREG2, VREGMEM). This solution was chosen in former projects to get an efficient energy transformation from the battery to the step-down output (2.1 V), and at the same time get a low noise supply at the regulated outputs. For increased efficiency of the power supply concept the domains 1.5V_UC and 1.5V_DSP can be connected now directly to the step-down converter while VREG2a/b are switched off. Therefore the output voltage of the step-down converter has to be reduced to 1.5 V by default from start-up on. This is done by using the Mozart Plus / Twigo 4 Plus as PMU.

A step-up converter generates 19.5 V for display and keypad backlight supply. Care must be taken to avoid to big voltage drop caused by currents drawn during start-up of the step-up converter and a TX burst.

10.1.3 Reference Section

The 100k resistor R1300 connected to RREF is used as current reference for the Power-ASIC and it must be 1% tolerance.

VDD_RTC is used for 32 kHz clock supply. In case the battery is removed, the clock is supplied by the 100 uF capacitor C1344 for around 1 min.

10.1.4 Low Drop-Out Regulators (LDO's)

All supply domains are supplied via LDOs, except for the backlight supply. The LDOs must have a 100nF capacitor on the input and a capacitor on the output to ensure stability. The output capacitor size is given in the Power-ASIC specification.
The RF1 and RF2 supply has an extra ferrite beat (L1320, L1303). This was inserted to reduce the noise on the RF supply.

10.1.5 DCDC Step-Down Converter

The power from the battery is fed to the PMU input VDDBUCK 1 and VDDBUCK2 through a Phi-type LC low pass filter build up with C1304, C1307, L1300, C1306-1 and C1306-2. This filter is required to suppress 900 and 1800 kHz noise generated from the step-down converter backwards to the battery. The current sense resistor R1302 is used for the coil current limitation. The component values of the output stage (V1302, L1301, C1354, C1359) are given by the Power-ASIC specification.

10.1.6 DCDC Step-Up Converter (backlight supply)

The power from the battery is fed to the switching circuit through the same Phi-type filter as used for the step-down converter (C1307, L1300, C1306-1 and C1306-2). This filtered voltage is named BATT_DCDC. The switching circuit is built up by L1302, the diode V1303, three capacitors C1355 and C1356 in parallel and a switching transistor. The capacitance of the used ceramic capacitor decreased with higher DC voltages (DC-biasing), so two 4u7 capacitors 1206 with 25 V in parallel must be used to reach the required capacity of 4u7 at 19.5 V output voltage.
The output voltage is determined by the resistive voltage divider from the output voltage VBOOST. The internal reference voltage is 1.25 V. The tolerance of the divider resistors has a big influence; therefore 1% resistors are used for R1340 and R1341. When the step-up converter is not in use the voltage divider is connected through V1303, L1302 and the noise filter directly to the battery. So the divider must be designed high resistive to keep the quiescent current as low as possible. Two parallel capacitors to the resistors increase the AC stability without increasing the quiescent current.

10.1.7 Illumination Control

The brightness control of the display and keypad LEDs works with the two PWM outputs, LIGHT_PWM1 and LIGHT_PWM2. With one of these signals a constant current sink, built up around the double transistor V2302 is controlled in duty cycle. The resistor R2311 determine the current approximately by I=0.6/R. At the moment the second current sink is replaced by a simple switching FET V2801 for the keypad illumination. This FET is a double FET, with one device shortened by R2859. So it acts as a single FET placed on the footprint of a double transistor. The LEDs of the keypad are connected to the battery voltage directly. In a later stage of the project this can be changed back to a common supply of display and keypad from the step-up, if for the PMU a Mozart+ VBOOST or the Twigo 4+ is used. In that case the step-up voltage can deliver more current than today the Mozart Plus, which is limited to round about 25 mA. This requires also changes in the external switching circuit.

10.1.8 Vibra Motor Supply

PWM mode: In this case the supply works as a step-down converter at 21 kHz. The speed of the vibra is easily controlled by changing the PWM in several steps.

The diode V2100 serves as ESD protection. In PWM mode it is also used for freewheeling when the vibra switch in the Power-ASIC is off. Because of this functionality it is necessary to use a Schottky diode, otherwise the negative voltage on the Power-ASIC VIBRA ball will exceed the permitted value.

10.1.9 Audio Amplifier

General Description

The audio part of the ASIC can be used with stereo single ended and with mono differential outputs. Both paths can be seen completely independent. It is possible to use different signals for mono and stereo in parallel. The following operating modes need to be supported:
Supply the speaker in the phone with audio signals including the possibility of hands-free and anti-pop switch on and off via the audio mono amplifier.
Supply of the headset with mono differential signals and with audio performance via the audio stereo amplifier.
Supply the speaker in the phone with ringing signal.
Transfer a key click, generated in digital part to the speaker.
Fast start-up with ringer time constant, but with audio multiplexer possibility for stereo and for mono mode.

Both audio amplifiers are adjustable by gain via TWI/SSC register separately.

Audio Mono Amplifier

The audio mono mode is done with a differential signal with the speaker as external load. The differential signal allows the maximum power, also in low voltage mode. The supply for the audio mono amplifier is VREGA. Only the last output stage is supplied by the battery.
Both amplifier paths are inverting amplifiers with external AC coupling at the input to compensate input offset. The gain of the amplifier is controllable over the TWI/SSC register separate for each channel in 1.5 dB steps from 21 dB to -54 dB and in 3 dB steps from -54 dB to -75 dB.
The output stage of the amplifiers can drive a low impedance load for the hands-free application. To guarantee an 'ANTI-POP' behaviour for switch on and off, a soft start-up with symmetrical ramp-up at each output is implemented.
In S68 the Mono Amplifier is used only to drive the speaker. The receiver will be driven from the S-GOLD2 to realise a double speaker concept to avoid acoustic shock.

Audio Stereo Amplifier

For stereo mode two single ended buffers are used. These buffers will be supplied by the additional regulator with 2.9 V to be more stable against the GSM ripple on the battery voltage. Also the reference voltage for the buffers is generated by a high precision, low noise band-gap reference for better performance.
An external capacitor is needed to filter this reference additionally. The gain steps for the programmable gain amplifier are identical with the mono amplifier. No key-click and ringer needed for the stereo part. Gain can be controlled with the TWI/SSC registers. The connected speaker has an impedance of typical 16Ohms. To guarantee an ANTI-POP noise a digital start-up is implemented. This will allow a soft start of the VMID and creates a "clean" audio band during the start-up. To eliminate the external coupling capacitor for the speaker, a 3rd amplifier was added. This amplifier creates the virtual ground node for both speakers. Therefore the current capability must be two times of the regular output amplifier. The purpose of this amplifier is to define the DC operating point with no DC current. The gain of the amplifier is controllable over the TWI register separate for each channel in 1.5 dB steps from 21 dB to -54 dB and in 3 dB steps from -54 dB to -75 dB.

Ringer Mode
In ringer mode the ringing signal is transferred directly as audio signal to the speaker. This architecture does not need an additional buzzer. The speaker is controlled with a rectangular signal created supplied by RINGIN pin. Input signal is a digital signal with variable frequency and comes from the S-GOLD2. The amplitude can be adjusted with register values. For start-up a smaller time constant must be used to allow a fast switch on behaviour. Ringing function can be started at any time.

Key-Click Function
It is possible to program a key-click to accompany each pushing of a key. A PWM signal with a selectable frequency is created and can be varied for the pulse width. The start-up is similar to the RINGER function. If the audio is off, the start-up is done with KEYCLICK time constant. If audio is starting with AUDIO start-up, the time constant is switched to KEYCLICK, too. If the audio amplifier is already up and running, the KEYCLICK is connected to the amplifier and audio signal is muted due to open multiplexer.

Audio Mono Fast
The audio fast mode is close to standard audio mode. The purpose of this mode is to allow an external ringer or key-click signal to be supplied to the mono amplifier via the audio multiplexer.

Audio Stereo Fast
The stereo fast mode is close to standard stereo mode. The purpose of this mode is to allow an external ringer or key-click signal to be supplied to the mono amplifier via the audio multiplexer.

Output Audio Multiplexer
The audio multiplexer will allow switching line inputs or DAC outputs to mono and stereo amplifiers. An inversion of the supplied audio signals can be done. This is necessary to convert the single line signal to a differential signal driving the speaker with the doubled output voltage in a bridge circuit. For this an analogue inverter in the multiplexer makes a phase shift of 180° of one channel. It is possible to do this phase shift also directly by the input signal or by a special function of the DAC.

10.1.10 Audio ADC and DAC

Clock Scheme
The Power ASIC receives the 26 MHz wave signal from the RF part and generates with a shaper and a PLL the 104 MHz master clock for the modulator and DSP.

Serial Audio I2S Interface
The audio interface is a bi-directional serial interface. The TX and RX path are independent. The I2S bus is a three-wire connection that handles two time-multiplexed data channels for the DAC and the ADC. The three lines are the clock, the serial data line and the word select line.

Audio DAC
For audio signals a 24 bit sigma delta converter with 5 bit feedback is implemented. The digital information is delivered via the I2S interface. To be able to work with all possible operating modes, the sampling frequency can vary from 8 kHz to 48 kHz. The performance of the audio output signal must be guaranteed over the full range the human ear is able to hear.

Audio ADC
The ADC is able to digitise analogue input signals in stereo with a resolution of 16 bit, with output to the I2S interface. A digital high pass filter is implemented, which can be bypassed. The signal path includes also two amplifier stages with programmable gains. Inverting amplifiers are used to reduce the offset.

ADC Audio Multiplexer
The audio multiplexer will allow the switching of each of the different input sources to the mono and stereo output signals and to the ADC. For the ADC the selectable sources are the MIC1 and MIC2 inputs from the internal microphone and MICE1 and MICE2 for the external microphone. Also the line inputs LINE 1 and LINE2 can be switched to the ADC. For the speaker and the headset the input can come either from the line inputs or from the DAC1 and DAC2. Additionally, a conversion from mono single ended to differential signals can be done. For this a selectable inverter is integrated.

TWI Interface
The TWI interface is an I2C-compatible two-wire interface with an additional interrupt pin to inform the S-GOLD2 about special conditions. The TWI bus interface is configured as a slave unit with 1bit int(), 1bit SDA(serial data) and 1bit SCL (serial clock). The data and the address of the register files are defined including read/write bit, control status bits and the data bits shown on the next pages. The TWI interface is asynchronous to the internal clock.

SSC Interface
The SSC interface enables high-speed synchronous data transfer between the S-GOLD2 and the PMU registers.
SCLK – Serial Clock Signal: As the SSC interface is configured as a slave only; this is an input pin to the SSC.
MTSR – Master Transmit Slave Receive: As the device operates as a slave this is an input pin.
MRST – Master Receive Slave Transmit: This is an output of the PMU used to transfer data to S-GOLD2 MRST input.
SSCSSEL – SSC Select, active low: This is an input to the PMU and is generated by the S-GOLD2 that it is controlling the PMU. When this signal is held low, data communication is enabled.

Charging Circuit
The charge voltage is detected by the signal VDD_CHARGE. A 100Ohms resistor R1353 is inserted between POWER and VDD_CHARGE. The purpose is to limit the current in case the polarity of the charge voltage is inverted by accident.
The DUAL-MOSFET for charging is controlled by the Power-ASIC via the CHARGE_CNTRL signal. The charge FET is either off, fully conducting or current controlled. R1344 is a current sense resistor and the voltage drop is fed into the Power-ASIC for current control and current supervision.
The phone can also supply external accessories from the battery via the charge circuit. In this case the MOSFET is fully on and the battery voltage appears at POWER pin of the accessory connector.

10.1.11 Battery

A Li-Ion Battery with a typical capacity of 690 mAh is used.
Under GSM-discharge conditions the battery will provide a discharge typical capacity of 660 mAh.
An internal safety circuit prevents from over-charging, over-discharging and over-current.

10.1.12 Charging

General

The battery is charged in the phone. The hardware and software is designed for LiIon with 4.2 V technology. Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging shall take place in the background (the customer can see this via the 'Charge' symbol in the display). During normal use the phone is being charged. Charging is enabled via a PMOS switch in the phone. This PMOS switch closes the circuit for the external charger to the battery. The processor takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the PMU hardware can override/interrupt the charging in the case of over voltage of the battery.
For controlling the charging process it is necessary to measure the ambient (phone) temperature and the battery voltage. The temperature sensor will be an NTC resistor with a nominal resistance of 22 kΩ at 25°C. The determination of the temperature is achieved via a voltage measurement on a voltage divider in which one component is the NTC.

Measurement of Battery voltage, Battery Type and Ambient Temperature

Measurement of Battery voltage, Battery Type and Ambient Temperature is done with an Analog to Digital Converter in S-GOLD2.

Timing of the Battery Voltage Measurement

In GSM talk mode the battery voltage is measured inside and outside (shortly before) the TX burst, otherwise it is measured outside TX slot only.

Recognition of the Battery Type

The different batteries will be encoded by different resistors within the battery pack itself.

Charging Characteristic of Lithium-Ion Cells

Li-Ion batteries are charged with a U/I characteristic, i.e. below the maximum voltage (4.2 V) the current shall be constant, after reaching the maximum voltage the average charging current has to be decreased in order to keep the unloaded voltage constant (4.2 V). The maximum charging current is given by the connected charger. The battery voltage must not exceed 4.2 V. During the charging pulse the voltage may reach 4.3 V. The temperature range in which charging of the phone may be performed is from 0...50°C. Outside this range no charging takes place, the battery only supplies current.

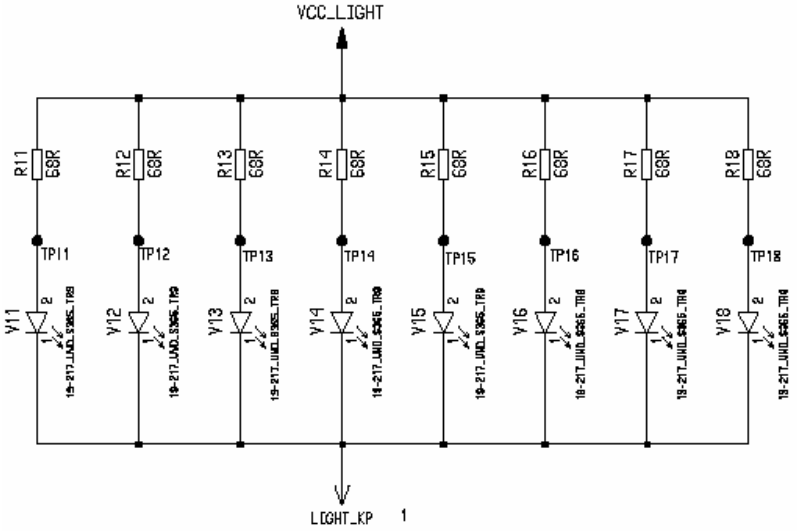
Trickle Charging
The PMU is able to charge the battery at voltages below 3.2 V without any support from the charge SW. The current will by measured indirectly via the voltage drop over a shunt resistor and linearly regulated inside the PMU by means of the external FET. The current level during trickle charge for voltages <2.8 V is in a range of 20-50 mA and in a range of 50-100 mA for voltages up to 3.2 V. To limit the power dissipation of the dual charge FET the trickle charging is stopped in case the output voltage of the charger exceeds 10 Volt. The maximum trickle time is limited to 1 hour. As soon as the battery voltage reaches 3.2 V the PMU will switch on the phone automatically and normal charging will be initiated by software.

Normal Charging (Rapid charge)
For battery voltages above 3.2 Volt and normal ambient temperature between 0 and 50°C (for start of charge a reduced range from 5°C to 45°C is applied) the battery can be charged with a charge current up to 1C. This charging mode is SW controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the PMU ASIC. The level of charge current is only limited by the charger. When the maximum voltage of 4.2 V with continuous current is reached the duty cycle is reduced in a way that a small pause is generated. During the pause the unloaded voltage is measured and is kept constant to 4.2 V. This is achieved by reducing the duty cycle correspondingly until the end of charge criteria is reached.

USB Charging
The PMU can support USB charging if USB charging is integrated in the charging software. If charge voltage is in the range 4.4 V to 5.25 V USB charging is ongoing. During USB charging only limited charging is possible. Charge current is limited to 400 mA for the main charging period. For top off charging the current level is reduced in 2 steps (300 mA, 150 mA).

11 Illumination

The illumination of the keypad is made by eight white LEDs, mounted on the MMI PCB. The LEDs are directly supplied by the battery voltage. To reduce the influence of the battery voltage to the illumination of the LEDs, the LEDs are regulated by PWM.



12 MMI

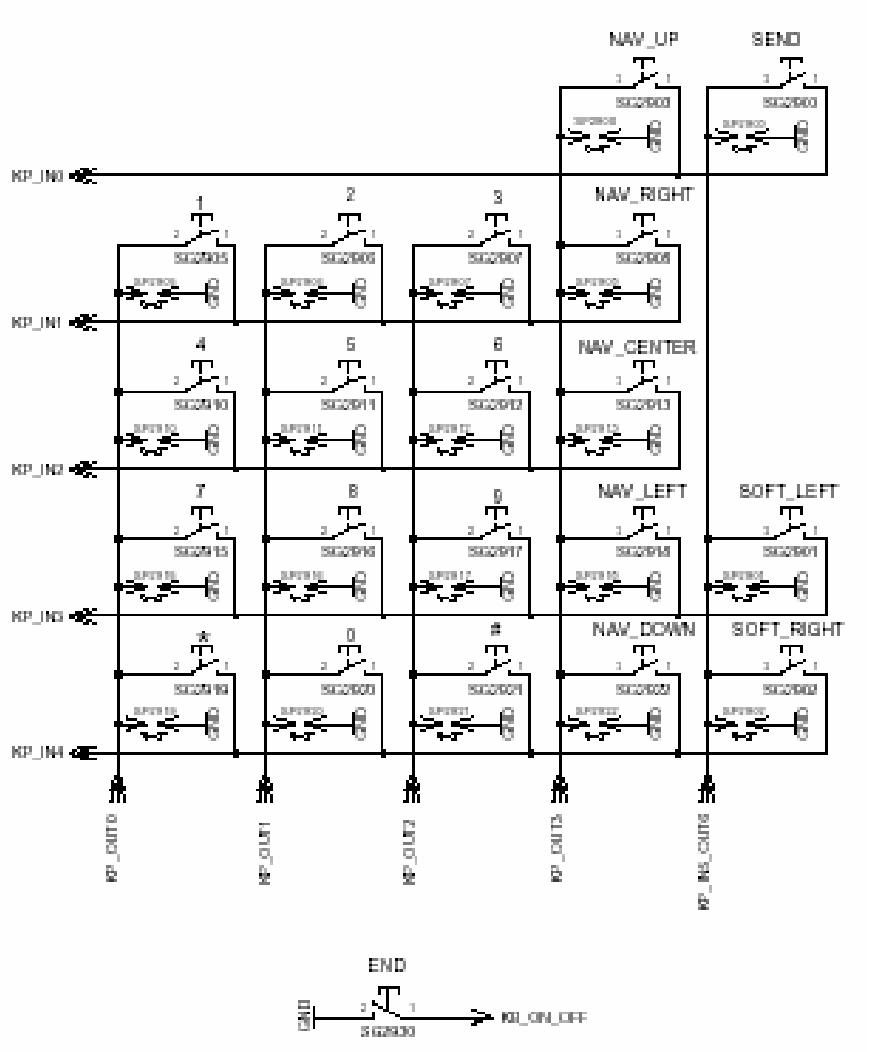
12.1 Keyboard

General description

The Keypad matrix consists of the keys ‘0’ to ‘9’, ‘*’, ‘#’, two soft keys, a 5-way navy key, a ‘SEND’, and an ‘END’ key.

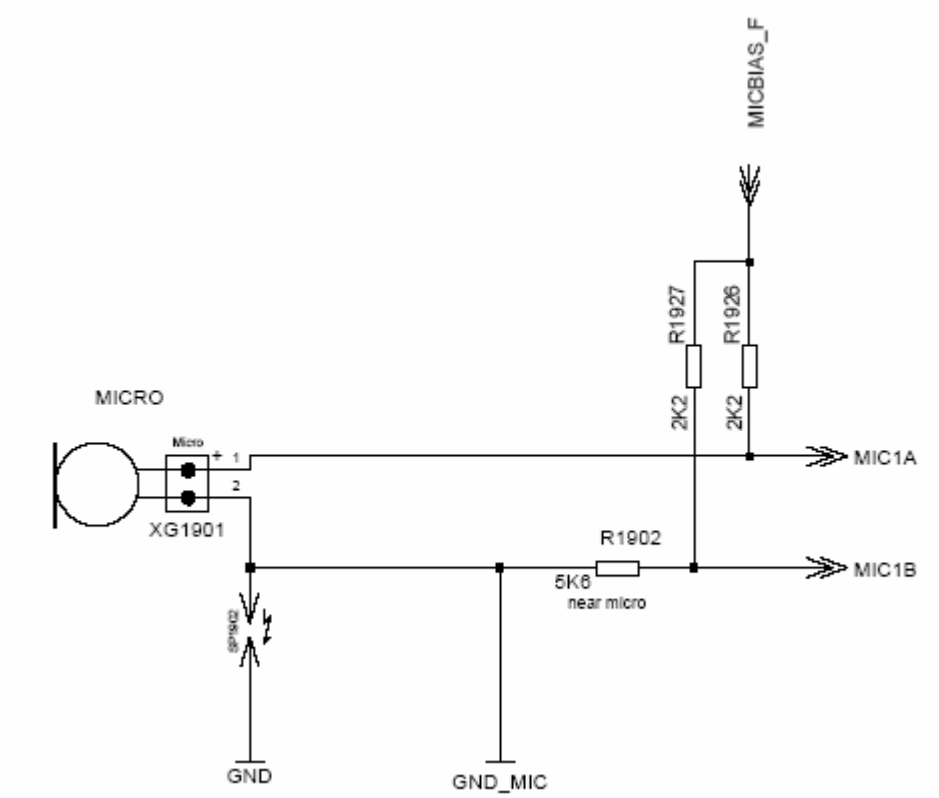
The keys are located at the MMI board.
In addition, four side keys are connected to the matrix. They are located on the main PCB
The ‘END’ key has a double-function. If the mobile phone is switched off and the ‘END’ key is supported via a resistor with RTC-Voltage. By pressing the key brings the voltage goes down to zero and the power supply ASIC switches on the mobile phone. If the mobile phone is ON, the ‘END’ key acts as a normal key same as the other ones. However, the ‘END’ key depressed for a longer time, then the software recognizes this and switches the power supply ASIC off via I²C commando.

Block Diagram



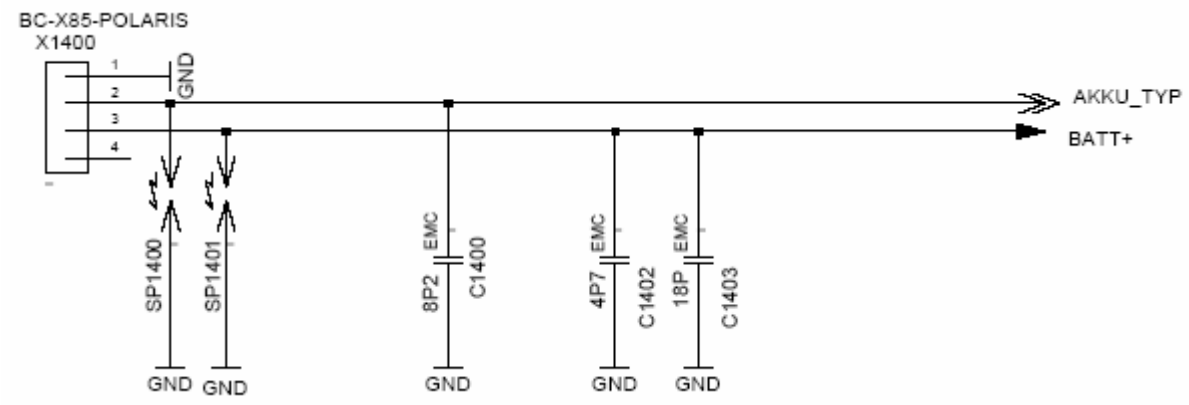
13 Interfaces

13.1 Microphone (XG1901)



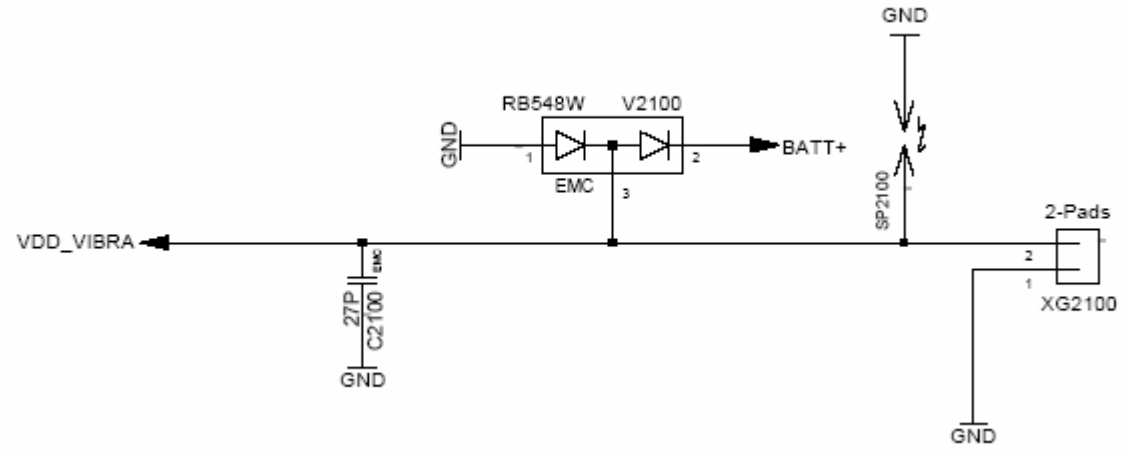
Pin	Name	IN/OUT	Remarks
1	MIC1A	O	Microphone power supply. The same line carries the low frequency speech signal.
2	MIC1B		GND_MIC

13.2 Battery (X1400)



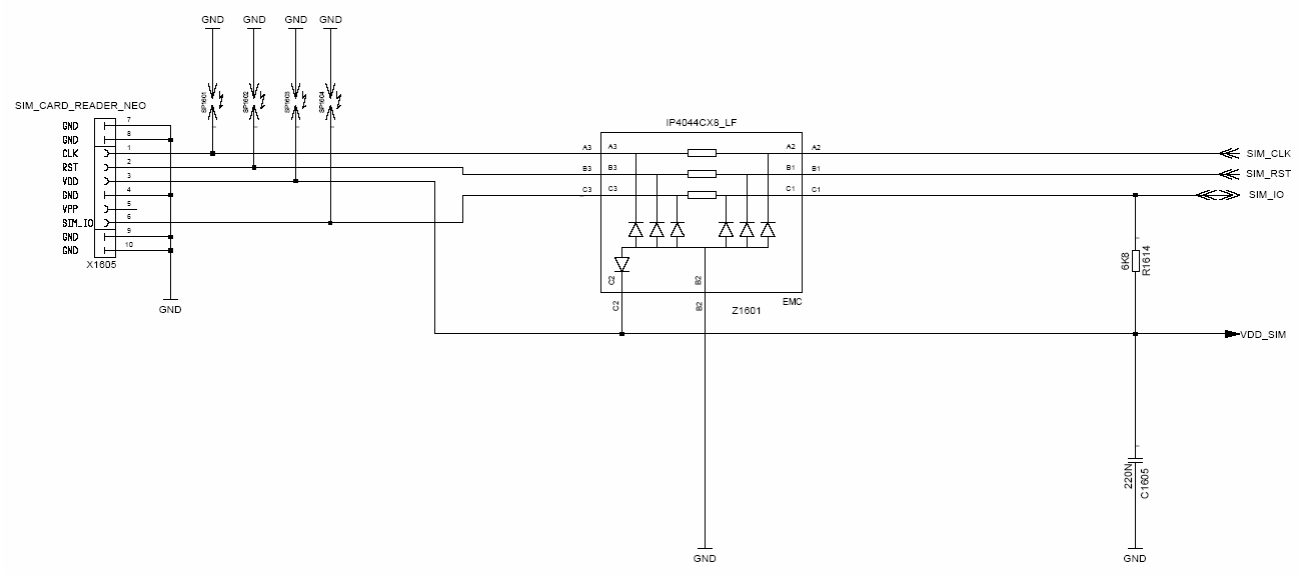
Pin	Name	Remarks
1	GND	Ground
2	AKKU_TYP	Recognition of battery/supplier
3	BATT+	Positive battery pole

13.3 Vibration Motor (XG2100)



Pin	Name	IN/OUT	Remarks
1	GND		
2	VDD_VIBRA		Vbatt will be switched by PWM-signal with internal FET to VDD_Vibra in Asic

13.4 Interface SIM Module with ESD protection

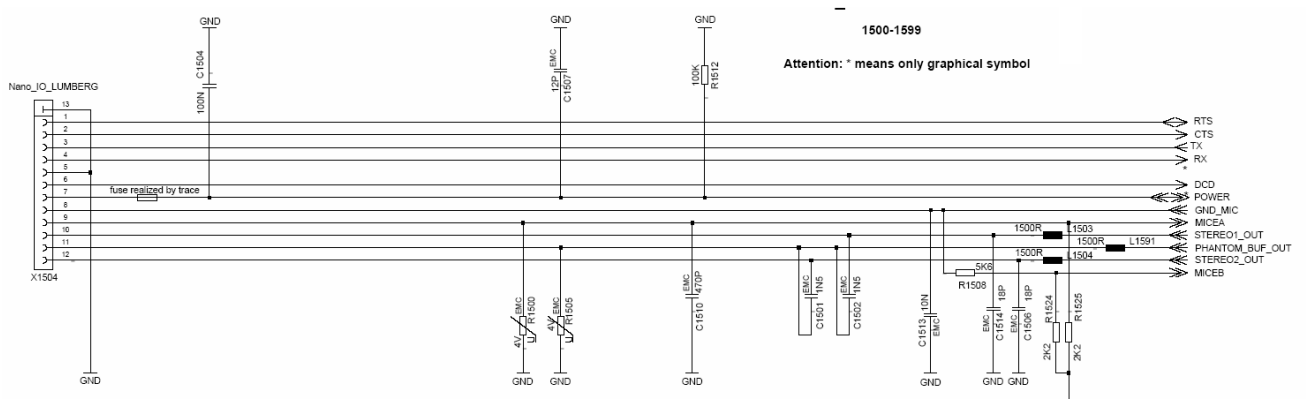


Pin Name	IN/OUT	Remarks
SIM_CLK	O	Pulse for chipcard. The SIM is controlled directly from the SGOLD.
SIM_RST	O	Reset for chipcard
SIM_IO	I/O	Data pin for chipcard
VDD_SIM	O	Switchable power supply for chipcard;

The Z1601 is a 3-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals. Additionally diodes are contained to protect downstream components from Electrostatic Discharge (ESD) voltages

13.5 Nano IO Connector with ESD protection

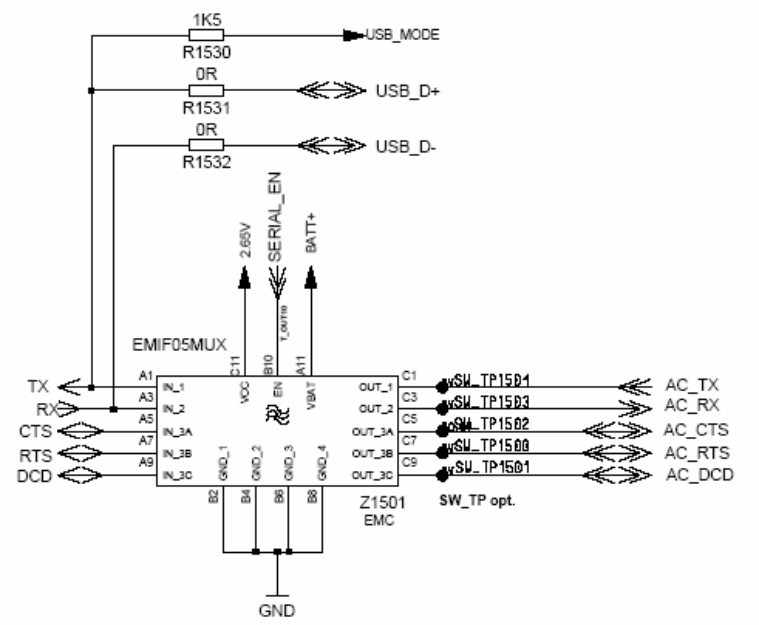
IO Connector



Pin	Name	IN/OUT	Notes
1	D+/RTS	I/O	Use as RTS in data-operation.
2	D+/CTS	I/O	Data-line for accessory-bus Use as CTS in data operation.
3	TX	O	Serial interface
4	RX	I	Serial interface
5	GND		
6	FLASH/DCD	I/O	Clock-line for accessory-bus. Use as DTC in data-operation.
7	POWER	I/O	POWER is needed for charging batteries and for supplying the accessories. If accessories are supplied by mobile, talk-time and standby-time from telephone are reduced. Therefore it has to be respected on an as low as possible power consumption in the accessories.
8	GND_MIC	Analog I	for ext. microphone driving ext. left speaker
9	MICP2	Analog I	External microphone
10	AUDIO_R	Analog O	driving ext. right speaker With mono-headset Audio_L and Audio_R differential Signal
11	AUDIO_REF	Analog O	mid-voltage in stereo mode refernce to AUDIO_L and AUDIO_R in mono mode not used
12	AUDIO_L	Analog O	driving ext. left speaker With mono-headset Audio_L and Audio_R differential mode

ESD Protection with EMI filter

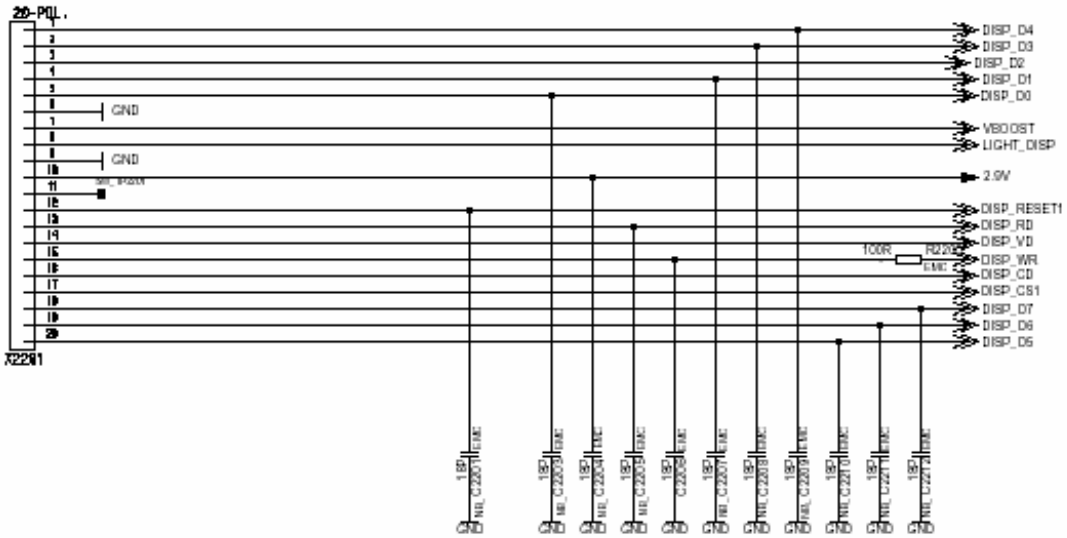
The Z1501 is a 5-channel filter with over-voltage and ESD Protection array which is designed to provide filtering of undesired RF signals in the 800-4000MHz frequency band Additionally the Z1501 contains diodes to protect downstream components from Electrostatic Discharge (ESD) voltages



13.6 Display Connector

DISPLAY_CONNECTOR

2200-2299



Pin Number	Pin Name	Description
1	D4	Data Line
2	D3	Data Line
3	D2	Data Line
4	D1	Data Line
5	D0	Data Line
6	GND	Ground
7	VBOOST	Power Supply for LED
8	LIGHT_DISP	LED Ground
9	GND	Ground
10	VDD	Power Supply for Logic
11	GND	Ground
12	XRES (RS)	Initialized when XRES is set to “L”
13	XRD	Read signal
14	TD (VE)	Synch Pin to avoid tearing effect
15	XWR	Write signal
16	A0 (CD)	Data command select signal
17	XCS	Chipset signal
18	D7	Data Line
19	D6	Data Line
20	D4	Data Line

14 S68 Diagram Sets

Double click the tag symbol to open the files.

TD_Repair_S68 Diagram Set_R1.0.pdf

TD_Repair_S68_Logic Diagram_R1.0.pdf

TD_Repair_S68_RF_ HIT_Diagram_R1.0.p